IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Gurtej S. Sandhu

Serial No.:

Filed: November 9, 2001

For: METHOD TO FORM ETCH AND/OR CMP STOP LAYERS

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§ Group Art Unit:
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§ Examiner:
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§ Atty. Docket: 98-1191.01
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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents

Washington, D.C. 20231

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I HEREBY CERTIFY THAT THIS PAPER IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 C.F.R. § 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO THE ASSISTANT COMMISIONER FOR PATENTS, WASHINGTON, D.C. 20231.

Susan Jerome
Signature

Dear Sir:

After awarding the above-captioned application the benefit of the priority date of its parent -- application #09/531,680, filed March 20, 2000 -- please amend the current application as follows.

IN THE SPECIFICATION:

Applicants are concurrently submitting a copy of the specification originally submitted in the parent application. Applicants are also submitting a clean substitute specification that includes the claims and is in the paragraph-numbered form requested by the Patent Office. The substitute specification contains no new matter. Applicants are further submitting a marked-up version of the substitute specification showing changes in relation to the specification originally submitted in the parent application.

IN THE CLAIMS:

Please cancel claims 1-16 and 79-88 without prejudice.

REMARKS

Claims 17-78 are the only claims pending as of this Preliminary Amendment. In a restriction required during prosecution of the parent application (see the Office Action of 3/23/01), the Examiner identified these claims as "Group II" claims "drawn to method of making a semiconductor device, classified in class 438, subclass 238." If there are any matters which may be resolved or clarified through a telephone interview, the Examiner is requested to contact Applicant's undersigned attorney at the number indicated.

Respectfully submitted,

Date: 11/8/1

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Appendix

Office Action dated 3/23/01
From prosecuting the parent application 09/531,680

DOCKET NO.: 98-01191.01

SUBSTITUTE SPECIFICATION
(MARKED VERSION)

FOR

METHOD TO FORM ETCH AND/OR CMP STOP LAYERS

INVENTOR(S):

Gurtej S. Sandhu

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A METHOD TO FORM ETCH AND/OR CMP STOP LAYERS

Related Application

[0001] This application is a divisional of application serial number 09/531,680, filed March 20, 2000.

Technical Field

[0002] ——The present invention relates generally to a doped non-conformal layer in a semiconductor device. More specifically, the present invention relates to a boron-doped oxide that can be used as a stopping layer for etching or chemical-mechanical planarization (CMP), among other uses.

Background of the Invention

[0001] ——The formation of semiconductor devices (which may actually include conductive and insulative materials as well as semiconductive elements) often involves removing amounts of material included as part of the device. Occasionally, the desired result of removing material is a planarized surface. Other times, the desired result is an opening extending at least partway into the material. Examples of both results occur in the manufacture of dynamic random access memory (DRAM) devices, wherein transistor gates are formed over a semiconductor substrate. Once the gates are formed, an insulator can be deposited between and over them. The surface of this insulator is lowered to the general level of the gate top and planarized through etching or CMP. After that, a contact opening is etched through the insulator to a doped region of the semiconductor substrate that forms a transistor source or drain. This opening will subsequently be filled with conductive material, thereby allowing electrical communication with the doped substrate.

[0002] ——This process of forming a hole within an insulation layer and filling that hole with a conductive material is generally known as a damascene process. Damascene processes offer an alternative to etching away undesired portions of a continuous conductive layer and surrounding the remaining portions with insulation. Damascene processes used at various fabrication stages provide additional examples of where material removal is desired in the context of DRAM devices. For example, initially providing the damascene insulation layer may involve CMP before the hole is formed therein, and forming the hole usually involves an etching step.

[0003] ——During CMP or etching steps such as those described above, it is often preferable to provide some sort of CMP stop or etch stop at a location defining the extent of the removal process. Oftentimes this CMP/etch stop will be some sort of material that is more resistant if not completely immune to the CMP/etch process than is the material that is to be removed. For example, United States Patent 5,485,035 by Lin et al. discloses using a first boron-doped oxide layer in carrying out a planarizing etch back (see Lin's Fig. 3) and a second boron-doped oxide layer to stop the via etch through an overlying insulating layer (Lin's Fig. 5).

[0004] Such oxides can be deposited by growing them from a surface in an oxidizing atmosphere or by conventional deposition methods, such as chemical vapor deposition (CVD). Another method of providing oxide is a process known as Flowfill. Flowfill involves reacting silane with vaporized hydrogen peroxide. The reaction results in a gas which condenses as a liquid on a substrate cooled to about 0°C. A subsequent heat treatment dries the liquid to form SiO_2.

[0005] As for the application of Flowfill-created oxides, prior art discloses a CMP process that stops within a Flowfill layer, although it is unclear from one particular reference whether this is a matter of properly timing the CMP or due to some property of the oxide itself. *See* Sabine Penka, *Integration Aspects of Flowfill and Spin-on-Glass Process for Sub-0.35μm Interconnects*, PROCEEDINGS OF THE IEEE 1998

INTERNATIONAL INTERCONNECT TECHNOLOGY CONFERENCE, at 271 (1998). Significantly, this reference further specifies that "Flowfill . . . need[s] to be enclosed by a base and a cap oxide." Other references further emphasize the presence of a base and cap. See, e.g., U. Höckele, et al., *Flowfill-Process as a New Concept for Inter-Metal-Dielectrics*, MATERIALS SCIENCE FORUM, at 235 (1998); A. Hass Bar-Ilan et al., *A comparative study of sub-micron gap filling and planarization techniques*, PROCEEDINGS OF THE SPIE – THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING, at 278-279 (1995); K. Beekmann et al., *SUB-MICRON GAP FILL AND IN-SITU PLANARISATION USING FLOWFILL™ TECHNOLOGY*, at 137 (1996). The base layer is an oxide provided by plasma-enhanced CVD (PECVD) and serves as an adhesion layer for the Flowfill oxide.

[0006] Concerning altering the properties of Flowfill layers, U.S. Pat. No. 5,985,770, also assigned to Micron Technology Inc., discloses gas phase doping of a Flowfill layer before or during the heat treatment that ultimately solidifies the Flowfill liquid into SiO_2.

[0007] ——Given the state of the prior art in terms of CMP and etch stops, there is a constant need in the art to find a new etch stop or CMP stop and new ways of making them. Moreover, there is also a need in the art to find new applications for and modifications of the Flowfill process.

Summary of the Invention

[0008] ——Accordingly, exemplary embodiments of the current invention provide a doped non-conformal oxide. In a preferred exemplary embodiment, a non-conformal oxide that resists doping is initially provided by way of a Flowfill process. Next is provided a second non-conformal oxide that is configured to accept dopant more readily. Subsequently the second oxide is annealed in an atmosphere containing boron. Alternative method embodiments include other ways of flowing at least one of

the oxides. Still other alternatives address other ways of providing non-conformal oxides, such as through a high-density plasma CVD. Yet other alternative exemplary embodiments address the use of a doped non-conformal oxide as an etch stop and/or a CMP stop.

Brief Description of the Drawings

[0009] —FIG. 1 depicts a cross section of an in-process DRAM as known in the prior art.

[0010] —FIGS. 2-11 illustrate cross-sections of an in-process DRAM having undergone steps in exemplary method embodiments of the current invention. These figures also show various exemplary apparatus embodiments within the scope of the current invention.

[0011] FIG. 12 illustrates a modified damascene process included as an exemplary embodiment of the current invention.

[0012] FIG. 13 shows a cross-section of an in-process semiconductor device portion having undergone steps included in another exemplary embodiment of the current invention.

[0013] FIG. 14 shows a cross-section of an in-process semiconductor device portion having undergone steps included in an alternative exemplary embodiment of the current invention.

[0014] FIG. 15 is a cross-section of an exemplary apparatus embodiment of the current invention.

[0015] FIG. 16 is a cross-section of another exemplary apparatus embodiment of the current invention.

[0016] FIG. 17 is a cross-section of still another exemplary apparatus embodiment of the current invention.

[0017] FIG. 18 shows a cross-section of an in-process semiconductor device portion having undergone steps included in yet another exemplary embodiment of the current invention.

Detailed Description of the Preferred Embodiment

[0018] ——FIG. 1 depicts a portion of a wafer in the process of having DRAM devices formed thereon. Specifically, FIG. 1 shows two transistor gates 20 flanked by insulating spacers 22. The gates 20 may include one or more conductive layers and an insulating cap. Further, the transistor gates 20 are over a gate oxide 24 which, in turn, overlies a substrate 26. In the current application, the term "substrate" or "semiconductor substrate" will be understood to mean any construction comprising semiconductor material, including but not limited to bulk semiconductive materials such as a semiconductor wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). Further, the term "substrate" also refers to any supporting structure including, but not limited to, the semiconductive substrates described above.

[0019] FIG. 2 illustrates a step taken as part of an exemplary method embodiment of the current invention. A first oxide 28 is provided over the transistor gates. Preferably the first oxide 28 is provided by the Flowfill process mentioned above. More specifically, the first oxide 28 is provided by reacting silane (SiH_4) with hydrogen peroxide (H_2O_2) at a pressure of about 1 Torr, a substrate temperature of 0°C, an SiH_4 flow rate of about 100 sccm, and an H_2O_2 flow rate of about 0.6g/minute. The result is silanol ($Si(OH)_4$) – a liquid that flows over the cooled substrate. Once deposited, heating the liquid $Si(OH)_4$ to about 450°C forms solid

SiO_2. As a result of this process, the first oxide 28 not only deposits on top of the gates 20 but also between them. However, the first oxide 28 is non-conformal in that horizontal portions are thicker than non-horizontal portions. Of further note is that this Flowfill process is used without necessarily providing an adhesion layer. In addition, the use of SiH_4 results in an oxide that will not readily accept dopant.

[0020] ——FIG. 3 illustrates that a second oxide 30 is subsequently deposited over the first oxide 28. Preferably, deposition occurs *in situ* -- in the same chamber as the previous oxide deposition. For this second oxide 30, it is preferred to react methylsilane -- H_3SiCH_3 -- with hydrogen peroxide -- H_2O_2 -- under parameters similar to those described above. The result is a flowable material (plus organic by products). This material can be considered an oxide precursor in that it forms SiO_2 after being heated to about 450°C. Accordingly, such a thermal treatment is carried out, thereby forming the second oxide 30. Like the first oxide 28, second oxide 30 deposits non-conformally with respect to the underlying surface. For example, in the exemplary embodiment pictured, the thickness of the second oxide 30 over a particular horizontal surface is generally constant given the self-planarizing nature of the deposition. Regarding non-horizontal surfaces, the second oxide 30 will vary in thickness and, in fact, may not deposit at all on some non-horizontal surfaces. Acceptable exemplary thicknesses for the second oxide 30 in this embodiment include 500 to 1000 Angstrom-thick horizontal portions and 0-50 Angstrom-thick non-horizontal portions. Thus, in at least some embodiments, the location of the second oxide 30 is limited to discrete portions of the underlying support structure or structures.

[0021] Unlike the first oxide 28, this second oxide 30 is porous and will readily accept dopant. Without limiting the current invention, it is believed that this second oxide 30 will do so because of its porous nature. As for the creation of these pores, it is thought that the formation process described above results in gaps within the second oxide 30 that are bigger than the lattice constant defined by the Si-O bonds of

that layer. These gaps, which may define lengths of 10 to 20 Angstroms and greater, may accommodate a dopant that is supplied in a later step. Accordingly, the term "pore" as used in this application, including the claims, is defined as a gap in a material, wherein the gap is bigger than the lattice constant of that material.

[0022] ——Accordingly, the second oxide 30 is subsequently doped with boron 32, the result of which is seen in FIG. 4. One way of doping is to anneal the second oxide 30 in an atmosphere containing boron. Exemplary parameters for such an anneal include an atmosphere wherein diborane (B_2H_6) contributes at least a partial pressure of the ambient; a temperature of 400-800°C; a pressure ranging from 0.5 Torr to 760 Torr; and a process time ranging from 10 seconds to 5 minutes. The first oxide layer 28 prevents most if not all diffusion of boron into other portions of the in-process DRAM device.

[0023] ——Next, an insulation layer 34 seen in FIG. 5 is layered over the in-process DRAM. This insulation layer is preferably formed of a glass such as borophosphosilicate glass (BPSG). The deposition of BPSG is a somewhat conformal process, resulting in an insulation layer 34 having a non-planarized surface 36. To achieve the desired planarized surface for that layer 34, a CMP process known in the art may be enacted. The portions of second oxide 30 atop the transistor gates 20, being harder to planarize than the overlying insulation layer 34, act as a CMP stop layer. The result, seen in FIG. 6, is an insulation layer 34 having a planarized surface 36' at the level defined by the second oxide 30 atop the gates 20.

[0024] ——Moreover, the lower portions of the second oxide 30 may also serve to stop another removal process. For example, it may be desired to provide a contact between the transistor gates 20. To do so, FIG. 7 illustrates that a layer of photoresist 38 is deposited over insulation layer 34 and patterned to expose a contact site 40. A subsequent etching step removes the insulation layer 34 material from contact site 40 yet has greater difficulty in removing the second oxide 30 near the bottom of the

contact site 40, as seen in FIG. 8. As an example, the in-process device can be exposed to a low-pressure HF vapor or a buffered HF solution at 23°C, which will etch BPSG to a greater degree than the boron-doped second oxide 30. The second oxide 30 may then be removed by a second etch. This second etch may take place in the form of another wet etch using HF. Alternatively, a reactive sputter etch or a plasma etch may be performed using gases such as CHF_3, CF_4, and C_2F_6. Exemplary plasma etch parameters include using CF_4 at a flow rate of 50 sccm, CHF_3 at a flow rate of 50 sccm, argon at a flow rate of 1000 sccm, a chamber pressure ranging from 0.2 to 0.002 torr, and an RF power of 750 W, for a time necessary to sufficiently remove enough of the second oxide 30. This etch may be used to remove the first oxide 28 and gate oxide 24 as well. Alternatively, separate etch steps may be applied to these oxides. Subsequent processing steps known in the art may be carried out to complete the DRAM.

[0025] ——The subsequent processing steps, however, may lead to other exemplary embodiments involving a non-conformal boron-doped oxide. FIG. 9 illustrates that a polycrystalline plug 50 is eventually deposited within the contact site 40. Assuming the in-process DRAM device will be incorporating capacitors using high-K dielectrics, it will be preferred to recess the plug 50 so that its surface does not reach the top of the contact site 40. As shown in FIG. 10, a non-conformal insulator 52, which can be formed in a manner such as that used to form the second oxide 30 above, may be deposited and doped with boron. Thereafter, a damascene process may be used to define a container in which a capacitor will appear. For example, a layer of insulation 54 as shown in FIG. 11 can be deposited and etched according to a patterned mask (not shown), with the non-conformal insulator 52 used to stop that etch. An additional etch may then be used to clear the boron-~~doped non-~~doped non-conformal insulator 52 from above the plug 50. However, this etch is optional. Regardless of whether this optional etch is performed, processing may continue, including steps that provide a capacitor within the container.

[0026] ——FIG. 12 demonstrates that non-conformal etch stops apply to other damascene-created structures as well. In that figure, an oxide layer 42 has been deposited over a support surface 44 (assumed to be a BPSG layer) and subsequently annealed in a boron-containing atmosphere. An insulating layer 46 is then deposited thereover and patterned according to a mask (not shown) to form an opening 48 configured to receive a conductive material. The etch process used to form the opening 48 will generally stop once the oxide layer 42 is reached.

[0027] ——The current invention also includes within its scope exemplary embodiments wherein the doped non-conformal oxide is used for purposes other than stopping etching or CMP. In FIG. 13, for example, a non-conformal oxide 56 has been deposited onto the surface of a material 58 and at the bottom of a trench 59 defined by that material 58. The material 58 is assumed to be BPSG but could be another material. Annealing the non-conformal oxide 56 in diborane using the parameters discussed above implants boron 60 into the non-conformal oxide 56. Further annealing of that oxide 56 can drive the boron 60 into adjacent regions 62 of the material 58. The non-conformal oxide 56 may then be removed, leaving a trench 59 having a doped bottom and substantially undoped sides, and the material 58 around the trench 59 having a doped surface.

[0028] ——Alternatively, if it is not desired to dope the surface of material 58, a barrier layer 64 such as a nitride may be deposited before etching the trench 59. The result after annealing the boron-doped non-conformal oxide 56 is depicted in FIG. 14. Yet another alternative is to remove the doped surface by way of a planarization step, such as CMP, performed before annealing.

[0029] Still another alternative is to provide process parameters such that the deposition of the non-conformal oxide on the top of the material 58 is reduced or perhaps even eliminated. For example, if methylsilane is reacted with hydrogen peroxide at room temperature (about 20°C), then the non-conformal oxide 56 will be

thicker at the bottom of trench 59 than amounts, if any, at the top, as seen in FIG. 15. Further, it is also believed that, as the temperature during deposition approaches 100°C, the non-conformal oxide will deposit a thicker amount on the surface than at the bottom of a trench 59 in that surface, an extreme result of such being depicted in FIG. 16. Thus, as seen in FIG. 17, the current invention includes within its scope exemplary embodiments wherein a non-conformal doped oxide has different thicknesses on a first horizontal surface 100, a second horizontal surface 200, and a non-horizontal surface 300 of a device, wherein such thicknesses are determined by process parameters including the ones addressed above. Further, the thickness at any of these regions may be reduced to zero.

[0030] ——In other cases, it may simply be desired to fill a trench 65 with a doped oxide, and embodiments of the current invention can accommodate such cases. A non-conformal oxide 66 can be deposited and subsequently doped, using, for example, the methylsilane deposition/diborane anneal steps discussed above. The result is seen in FIG. 18. The oxide 66 can be subsequently etched or CMP'd to make the oxide 66 generally level with the surface of support material 68. Currently, borosilicate glass (BSG) is deposited in such trenches by way of conventional means, but as trenches become narrower in width, standard BSG deposition methods may not work. Thus, this exemplary embodiment offers an alternative method for filling trenches with a boron-doped insulator. In fact, the boron-doped insulator in this and other exemplary embodiments could be considered to be a low dielectric constant (low-K) BSG, wherein a low dielectric constant is considered to be at most 3. Accordingly, exemplary embodiments of the current invention have applications in other contexts where BSG or other low-K dielectrics are used. For example, a doped non-conformal oxide could be used as an interlayer dielectric (ILD).

[0031] ——In addition, while it is preferred to deposit the oxide by heating the product of a methylsilane/hydrogen peroxide reaction, the current invention includes within its scope exemplary embodiments that provide a non-conformal oxide by other ways.

For example, another way to flow the oxide onto the underlying layer is through a spin-on-glass (SOG) process. The SOG process involves depositing a suspension of glass particles in an inorganic carrier onto a spinning substrate. Conventional photoresist tools can be used to achieve such a deposition. The organic carrier is then driven off of the substrate using a thermal process, and the remaining glass is reflowed to fill spaces in the underlying topography and to planarize the glass surface.

[0032] Another way of providing a non-conformal oxide is through the use of a high-density plasma (HDP) CVD process. In such a process, plasma gases including silicon-containing, oxygen-containing, and nonreactive gasses (e.g. a noble gas) are used to deposit an oxide while simultaneously etching the oxide to prevent gaps from forming in the oxide material. The density of the plasma is greater than 10^{10} ions per cm^3. Exemplary parameters include an ambient of O_2 (flowed at a rate of 120-500 sccm), SiH_4 (flowed at a rate of 80-250 sccm), and Ar (flowed at a rate of 0-50 sccm); an RF bias at 13.56 MHz; a temperature ranging from 350~~-700°C;~~ 700°C; and a bias power ranging from 0 to 2000 W. Moreover, other CVD processes could be used to provide a non-conformal layer.

[0033] ——In addition, it is not necessary that the dopant be boron. Exemplary embodiments of the current invention include those in which at least one other impurity replaces or is added along with boron. It is noted that U.S. Pat. No. 5,985,770 discussed above discloses doping the oxide precursor with various materials before and during formation of the oxide layer. For example, application '987 indicates that phosphorous doping can be accomplished using PH_3, phosphates, or phosphites; fluorine doping can involve NF_3 or F_2; carbon may serve as the dopant using C_2H_6, trimethyl silane ($(CH_3)_3SiH$) or CH_4; and nitrogen may dope the oxide using NF_3 or NH_3. The current invention includes within its scope exemplary embodiments that involve doping a non-conformal oxide after its formation with the dopants above (either alone or in combination) by using precursor gases such as the ones above (again either alone or in combination). More specific exemplary

embodiments include doping one portion of the non-conformal oxide with a first dopant and a second portion of the oxide with a second dopant. Appropriate masking of the portions can be used to allow for such selective doping.

[0034] —Furthermore, in embodiments wherein a diffusion barrier layer (such as the first oxide 28) is preferred, it is not necessary that the diffusion barrier be deposited in a non-conformal manner. Other exemplary embodiments allow for the barrier layer to be provided through standard methods resulting in a conformal layer. For example, an SiO_2 barrier layer could be provided under known conformal CVD parameters. Alternatively, a conformal layer of tetraethylorthosilicate (TEOS)-based glass could be layered before the non-conformal layer is provided and subsequently doped.

[0035] Given the variety of alternative embodiments described above, one skilled in the art can appreciate that, although specific embodiments of this invention have been described above for purposes of illustration, various modifications may be made without departing from the spirit and scope of the invention. Returning to the first exemplary embodiment described above, for instance, the first oxide under the doped second oxide is preferred to help prevent diffusion into other portions of the DRAM. However, the first oxide is not required, as careful processing can dope the second oxide without having the dopant diffuse beyond the oxide. Thus, embodiments without the first oxide fall within the scope of the invention. Further, as an addition to or an alternative to the preferred monomethylsilane/peroxide reaction, the current invention includes within its scope the use of other chemicals to provide a non-conformal oxide, including (but not limited to) dimethylsilane, trimethylsilane, tetramethylsilane, pentamethyldisilane, and combinations of chemicals. Moreover, while exemplary embodiments of the current invention have been illustrated in the context of a DRAM, these and other embodiments apply to semiconductor devices in general. Accordingly, the invention is not limited except as stated in the claims.

Claims

What is claimed is:

1. A memory device, comprising:

a circuit device defining a horizontal surface and a non-horizontal surface; and

a porous oxide over said circuit device, said porous oxide having a first thickness extending perpendicularly from said horizontal surface and a second thickness extending generally perpendicularly from said non-horizontal surface, wherein said second thickness is different from said first thickness.

2. The memory device in claim 1, wherein said porous oxide comprises an oxide defining at least one pore.

3. The memory device in claim 2, wherein said porous oxide comprises a plurality of silicon atoms and a plurality of oxygen atoms, wherein said plurality of silicon atoms and said plurality of oxygen atoms define a lattice constant; and wherein at least one dimension of said at least one pore is greater than said lattice constant.

4. The memory device in claim 3, wherein said dimension of said at least one pore is at least 10 angstroms.

5. The memory device in claim 4, wherein said dimension of said at least one pore ranges from 10 to 20 angstroms.

6. The memory device in claim 4, further comprising a dopant in at least one pore.

7. The memory device in claim 6, wherein said dopant consists of a selection from boron, carbon, phosphorous, fluorine, nitrogen, and combinations thereof.

8. A portion of a semiconductor device, comprising:

a support surface defining at least two elevations within said semiconductor device; and

a doped insulator non-conformally over said support surface, wherein said insulator is thinner between two consecutive elevations of said support surface than said insulator directly over at least one of said consecutive elevations.

9. The portion of a semiconductor device in claim 8, wherein said doped insulator is non-continuously over said support surface.

10. The portion of a semiconductor device in claim 8, wherein said doped insulator is a boron-doped insulator.

11. The portion of a semiconductor device in claim 8, wherein said doped insulator is a doped oxide.

12. The portion of a semiconductor device in claim 8, further comprising an undoped insulator between said doped insulator and said support surface.

13. The portion of a semiconductor device in claim 12, wherein said undoped insulator is non-conformally over said support surface.

14. A material for a semiconductor device, comprising a boron-doped oxide on at least one horizontal portion of said semiconductor device more so than on a vertical portion of said device.

15. The material in claim 14, wherein said semiconductor device includes a layer defining a trench; wherein said at least one horizontal portion comprises a bottom of said trench; and wherein said vertical portion is a sidewall of said trench.

16. The material in claim 15, wherein said at least one horizontal portion further comprises a surface of said layer even with a top of said trench.

17. A method of processing an in-process semiconductor device, comprising:

non-conformally depositing an oxide over said in-process semiconductor device;

doping said oxide; and

depositing an insulator over said oxide.

18. The method in claim 17, further comprising:

initiating a removal of at least a portion of said insulator; and

halting said removal using said oxide.

19. The method in claim 18, wherein said initiating step comprises initiating an etching of said insulator; and wherein said halting step comprises using said oxide as an etch stop.

20. The method in claim 18, wherein said initiating step comprises initiating a planarization of said insulator.

21. The method in claim 20, wherein said step of initiating a planarization of said insulator comprises initiating a chemical-mechanical planarization of said insulator; and wherein said halting step comprises using said oxide as a CMP stop.

22. A method of providing oxide for an in-process semiconductor device, comprising:

depositing a first oxide over said in-process semiconductor device; and

non-conformally depositing a porous second oxide onto said first oxide.

23. The method in claim 22, wherein said step of depositing a first oxide comprises depositing said first oxide in a chamber; and wherein said step of non-conformally

depositing a porous second oxide comprises depositing said second oxide in said chamber.

24. The method in claim 22, wherein said step of non-conformally depositing a porous second oxide comprises reacting methylsilane with hydrogen peroxide.

25. The method in claim 22, wherein said step of non-conformally depositing a porous second oxide comprises reacting H_3SiCH_3 with H_2O_2.

26. The method in claim 25, wherein said step of non-conformally depositing a porous second oxide further comprises:

cooling said in-process semiconductor device to about 0°C before said reacting step; and

providing a temperature of about 450°C inside said chamber after said reacting step.

27. The method in claim 26, wherein said step of depositing a first oxide comprises reacting silane with hydrogen peroxide.

28. A method of providing a doped oxide, comprising:

flowing an oxide precursor over a portion of a semiconductor device;

forming an oxide from said precursor; and

subsequently annealing said oxide in an atmosphere containing a dopant.

29. The method in claim 28, wherein said annealing step comprises annealing said oxide in an atmosphere consisting of a selection of PH_3, a phosphate, a phosphite, NF_3, F_2, C_2H_6, trimethyl silane, CH_4, NH_3, B_2H_6, and combinations thereof.

30. The method in claim 29, wherein said annealing step further comprises annealing at a temperature ranging from 400 to 800°C, at a pressure ranging from 0.5 to 760 Torr, and for a time ranging from 10 seconds to 5 minutes.

31. A method of processing a surface of an in-process memory device, comprising:

providing said surface as part of said memory device using a non-CVD process;

flowing a material onto said surface;

turning said material into a first oxide; and

doping said first oxide.

32. The method in claim 31, wherein said step of providing said surface comprises providing a barrier oxide using a Flowfill process; and wherein said method further comprises blocking diffusion of a dopant from said first oxide using said barrier oxide.

33. The method in claim 32, wherein said step of doping said first oxide comprises:

doping a first portion of said first oxide with a first impurity; and

doping a second portion of said first oxide with a second impurity.

34. A method of providing an etch stop for a semiconductor device, comprising:

providing at least one support surface as part of said semiconductor device, said surface having a horizontal portion and a non-horizontal portion;

depositing an oxide onto said support surface, wherein said oxide has a uniform thickness on said horizontal portion and a variable thickness on said non-horizontal portion; and

doping said oxide.

35. The method in claim 34, wherein said depositing step comprises depositing said oxide by way of a CVD process.

36. The method in claim 35, wherein said depositing step comprises depositing said oxide by way of an HDP CVD process.

37. A method of providing a CMP stop for a semiconductor device, comprising:

providing an element of said semiconductor device, said element having a top and a side;

depositing an oxide over said element, wherein said depositing leaves more of said oxide on said top than on said side; and

annealing said oxide in a doping atmosphere.

38. The method in claim 37, wherein said step of depositing an oxide comprises:

flowing a precursor to said oxide over said element; and

heating said precursor.

39. The method of claim 38, wherein said step of depositing an oxide comprises depositing said oxide using a spin-on-glass process.

40. A method of selectively doping a circuit device material, comprising:

depositing an oxide over a first horizontal surface of said circuit device material to the exclusion of a vertical surface of said material;

introducing a dopant into said oxide; and

diffusing said dopant from said oxide into said material.

41. The method in claim 40, further comprising a step of depositing a diffusion barrier over a second horizontal surface of said material; and wherein said step of depositing an oxide further comprises depositing said oxide over said diffusion barrier.

42. A method of filling a trench included as part of a semiconductor device, comprising:

reacting methylsilane with hydrogen peroxide in a chamber containing said semiconductor device;

allowing a product from a reaction of said methylsilane and said hydrogen peroxide to at least fill said trench;

changing said product into a silicon oxide; and

heating said silicon oxide in a boron atmosphere.

43. A fabrication process for a DRAM including a semiconductor substrate, said process comprising:

depositing an undoped self-planarizing first oxide over an in-process device included as a part of said DRAM;

depositing an undoped self-planarizing second oxide over said first oxide; and

doping said second oxide.

44. The process in claim 43, further comprising:

depositing an insulation layer over said second oxide;

planarizing said insulation layer; and

using said second oxide as a planarization stop.

45. The process in claim 43, further comprising:

depositing an insulation layer over said second oxide;

etching an opening in said insulation layer; and

using said second oxide as an etch stop.

46. The process in claim 45, wherein said step of using said second oxide as an etch stop comprises using a portion of said second oxide over said substrate as said etch stop.

47. The process in claim 46, said step of etching an opening in said insulation layer comprises etching said insulation layer at a first etch rate; and wherein said step of using said second oxide as an etch stop comprises etching said second oxide at a second etch rate, wherein said second etch rate is less than said first etch rate.

48. The process in claim 47, wherein said step of etching said insulation layer comprises exposing said insulation to a selection of an HF vapor and an HF liquid.

49. The process in claim 48, wherein said step of etching said insulation layer comprises exposing said insulation to a buffered HF liquid having a temperature of about 23°C.

50. The process in claim 48, wherein said step of etching said second oxide comprises exposing said second oxide to said selection.

51. A damascene process, comprising:

providing a material over a semiconductor substrate, said material having a fluid property;

forming an oxide from said material in response to allowing said material to lose said fluid property;

providing an insulation layer over said oxide;

etching an opening in said insulation layer;

halting said etching with said oxide; and

depositing a conductive material within said opening.

52. The damascene process in claim 51, further comprising a step of removing at least a portion of said oxide after said halting step and before said depositing step.

53. The damascene process in claim 52, wherein said step of forming an oxide comprises:

forming said oxide onto a BPSG layer; and

doping said oxide before said step of providing an insulation layer.

54. The damascene process in claim 52, wherein:

said step of providing a material comprises depositing said material having a planar surface and defining at least two different thicknesses, wherein depositing said material occurs before providing said insulation layer; and

said method further comprises doping said oxide before providing said insulation layer.

55. The damascene process in 54, wherein said step of depositing said material comprises depositing said material over a gate and over a conductive plug next to said gate, wherein a top of said plug is lower in elevation than a top of said gate.

56. The damascene process in claim 55, wherein said etching step comprises etching using a selection of a reactive sputter process and a plasma process.

57. The damascene process in claim 56, wherein said etching step comprises plasma etching using a gas comprising fluorine, wherein said gas includes a selection of CHF_3, CF_4, and C_2F_6.

58. The damascene process in claim 57, wherein said plasma etching step comprises:

providing a chamber configured to accommodate said semiconductor substrate;

flowing CF_4 into said chamber at a rate of 50 sccm;

flowing CHF_3 into said chamber at a rate of 50 sccm;

flowing Argon into said chamber at a rate of 1000 sccm;

providing pressure of 0.2 to 0.002 Torr inside said chamber; and

providing 750 W of RF power to said chamber.

59. A method of forming oxide over a transistor gate and over a substrate extending laterally from under said gate, said method comprising:

forming an undoped first oxide over said gate and said substrate;

forming an undoped second oxide over said first oxide;

doping said second oxide after forming said second oxide;

depositing insulation over said second oxide after doping said second oxide;

initiating a removal of a portion of said insulation; and

stopping said removal with said second oxide.

60. The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a TEOS-based oxide.

61. The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a continuous silicon dioxide layer.

62. The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a first oxide that is thicker over said gate than lateral to said gate, and wherein said first oxide is thicker over said substrate than lateral to said gate.

63. The method in claim 62, wherein said step of forming an undoped first oxide comprises forming a non-porous first oxide.

64. The method in claim 62, wherein said step of forming an undoped second oxide comprises forming a second oxide that is thicker over said gate than lateral to said gate, and wherein said second oxide is thicker over said substrate than lateral to said gate.

65. The method of claim 64, wherein said step of forming an undoped second oxide comprises:

depositing 500 to 1000 Angstroms of said second oxide over said gate;

depositing 500 to 1000 Angstroms of said second oxide over said substrate; and

depositing 0 to 50 Angstroms of said second oxide lateral to said gate.

66. A method of depositing an interlayer dielectric, comprising:

providing a first level of a semiconductor device, said first level defining a topography and comprising insulation;

depositing BSG onto discrete portions of said topography, said BSG having a dielectric constant of at most 3; and

providing a second level of said semiconductor device over said BSG.

67. The method in claim 66, wherein said step of depositing BSG comprises:

depositing glass onto said topography, said depositing resulting in a planar surface of said glass; and

lowering a dielectric constant of said glass.

68. The method in claim 67, wherein said step of depositing glass comprises:

flowing a silicon oxide precursor over said topography; and

hardening said precursor into a silicon oxide.

69. The method in claim 68, wherein said step of lowering a dielectric constant of said glass comprises doping said silicon oxide with boron.

70. The method in claim 69, wherein said step of providing a first level of a semiconductor device comprises providing a first level further comprising at least one conductive structure.

71. A method of processing a portion of a device including a higher horizontal surface, a lower horizontal surface, and a non-horizontal surface, said method comprising:

providing an oxide in a non-conformal manner over said higher horizontal surface, said lower horizontal surface, and said non-horizontal surface; and

introducing an impurity into said oxide.

72. The method in claim 71, wherein said step of providing an oxide in a non-conformal manner comprises providing an oxide having a first thickness on said higher horizontal surface, a second thickness on said lower horizontal surface, and a third thickness on said non-horizontal surface, wherein said first, second, and third thicknesses are different.

73. The method in claim 72, wherein said step of providing an oxide comprises providing an oxide having a first thickness greater than said second thickness.

74. The method in claim 72, wherein said step of providing an oxide comprises providing an oxide having a second thickness greater than said first thickness.

75. The method in claim 74, wherein said step of providing an oxide in a non-conformal manner comprises reacting methylsilane and hydrogen peroxide in an environment including a substrate having a temperature of about 20°C.

76. The method in claim 75, wherein said step of providing an oxide comprises providing an oxide over a non-horizontal surface connecting said higher horizontal surface to said lower horizontal surface.

77. A method of forming a doped oxide over a substrate, comprising:

reacting a methylsilane with hydrogen peroxide proximate said substrate;

forming an oxide from a product of said methylsilane and said hydrogen peroxide; and

introducing a dopant into said oxide.

78. The method in claim 77, wherein said reacting step comprises reacting said hydrogen peroxide with a selection comprising dimethylsilane, trimethylsilane, tetramethylsilane, pentamethyldisilane, and combinations thereof.

79. A semiconductor device, comprising:

a first portion of doped porous oxide on a first surface of said semiconductor device, wherein said first portion of doped oxide has a first thickness; and

a second portion of doped porous oxide on a second surface of said semiconductor device, wherein said second portion has a second thickness different from said first thickness.

80. The device in claim 79, wherein said first surface defines a first plane at a first elevation, and wherein said second surface defines a second plane at a second elevation.

81. The device in claim 80, wherein said first surface defines a first horizontal surface, and wherein said second surface defines a second horizontal surface.

82. The device in claim 81, further comprising a third portion of doped porous oxide on a third surface of said semiconductor device, wherein said third portion has a third thickness different from said first and second thickness.

83. The device in claim 83, wherein said third surface defines a transition from said first surface to said second surface.

84. A material for a portion of a semiconductor device, wherein said portion defines a varying topography, said material comprising a boron-doped porous oxide having varying thicknesses over said portion.

85. The material in claim 84, wherein said oxide is thicker at a higher elevation of said portion than at a lower elevation of said portion.

86. The material in claim 85, wherein said oxide is thicker at a horizontal section of said portion than at a non-horizontal section of said portion.

87. The material in claim 86, wherein said oxide has a thickness of zero at at least a part of said non-horizontal section.

88. The material in claim 87, wherein said oxide has a thickness of zero at said lower elevation.

Abstract of the Disclosure

In a DRAM fabrication process, a first oxide is provided over a transistor gate and over a substrate extending from under the gate. The deposition is non-conformal in that the oxide is thicker over the gate and over the substrate than it is on the side of the gate. A second non-conformal oxide is provided over the first non-conformal oxide. The second oxide is annealed in a boron-containing atmosphere, and the first oxide prevents boron diffusion from the second oxide into the gate and substrate. The second oxide may then serve as an etch stop, a CMP stop, or both.

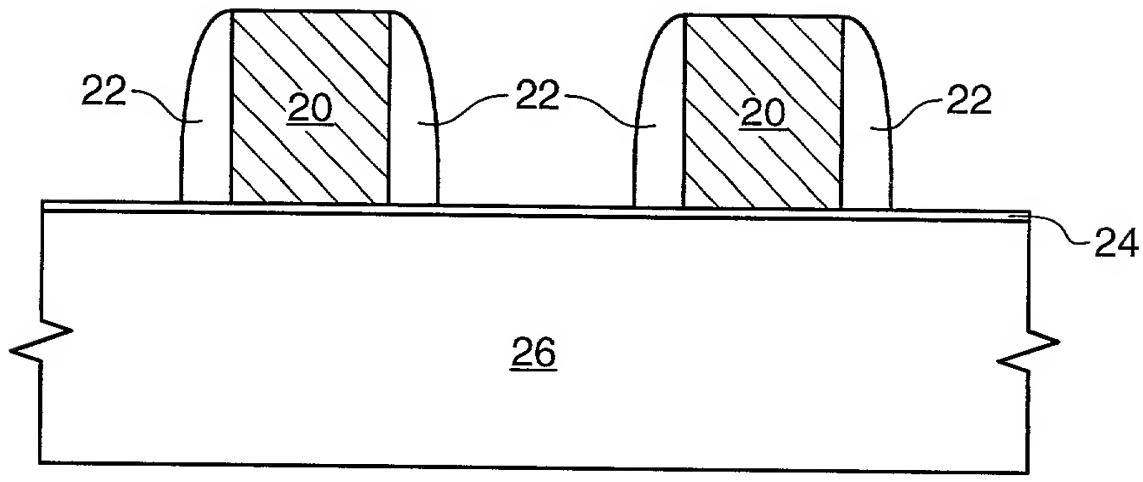

FIG. 1
(PRIOR ART)

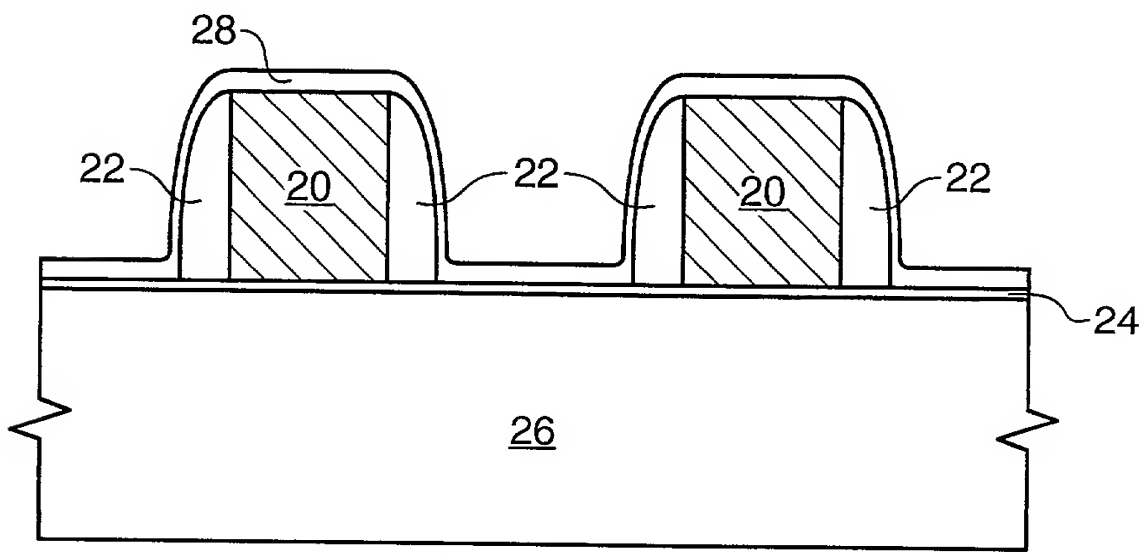

FIG. 2

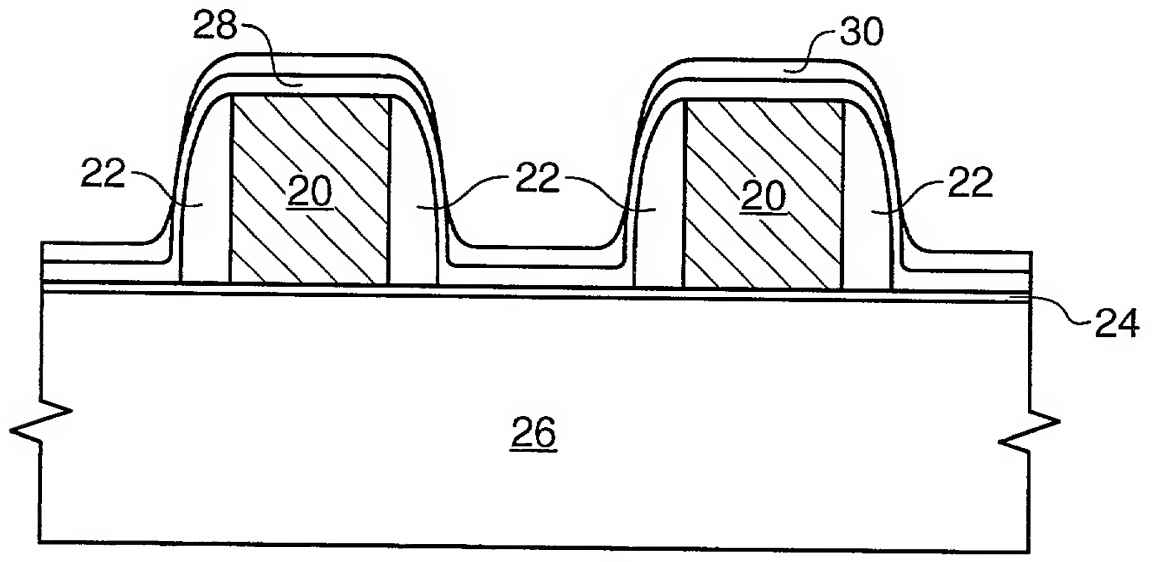

FIG. 3

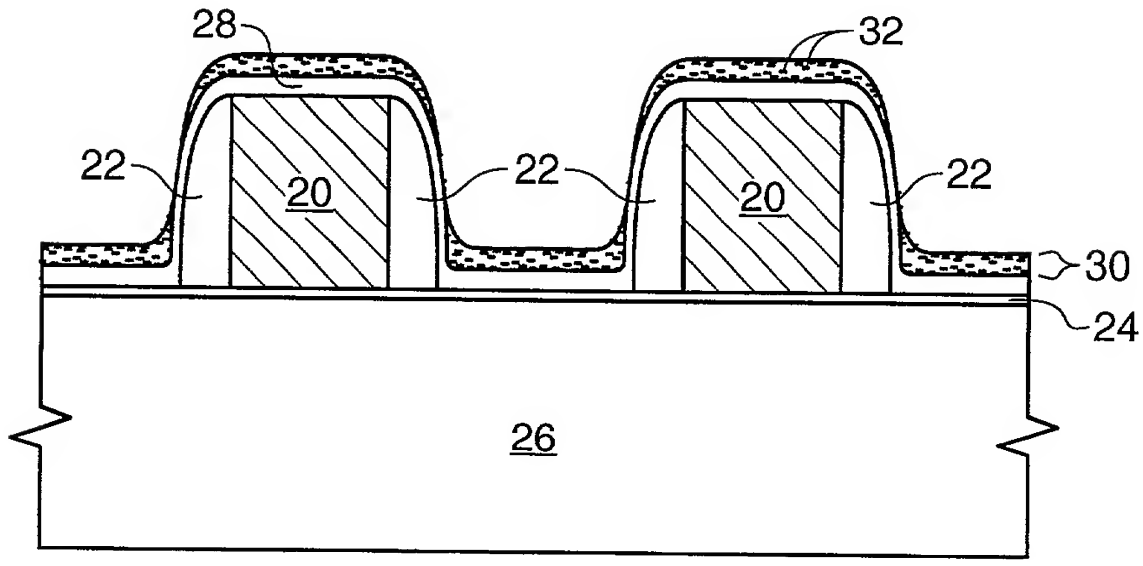

FIG. 4

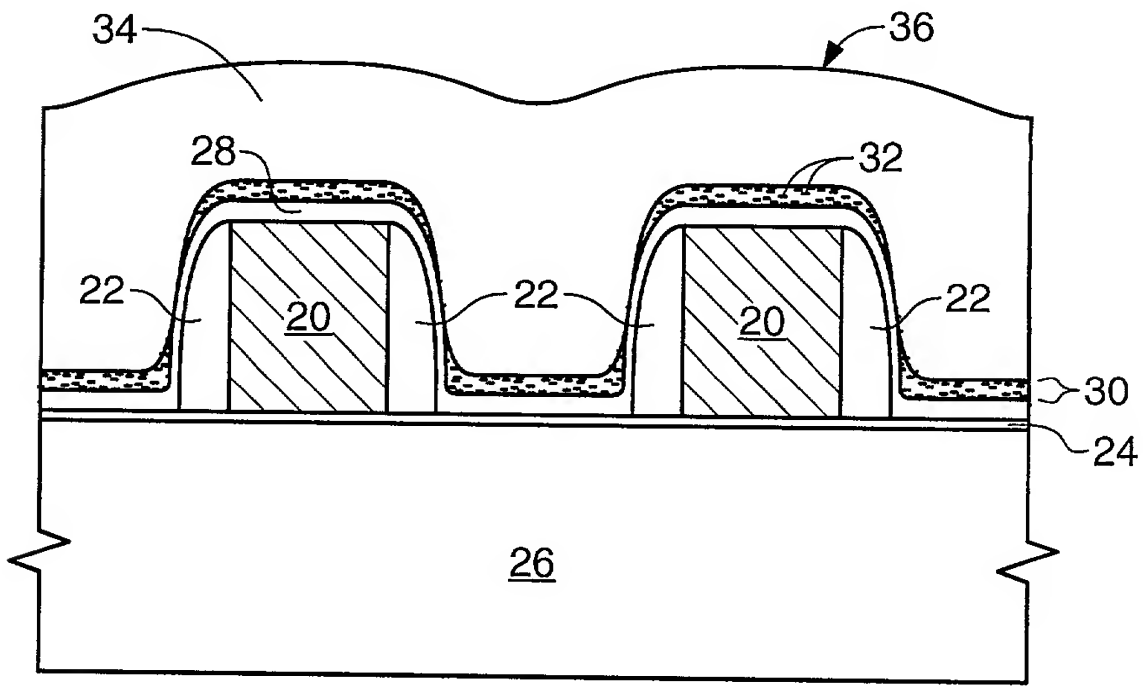

FIG. 5

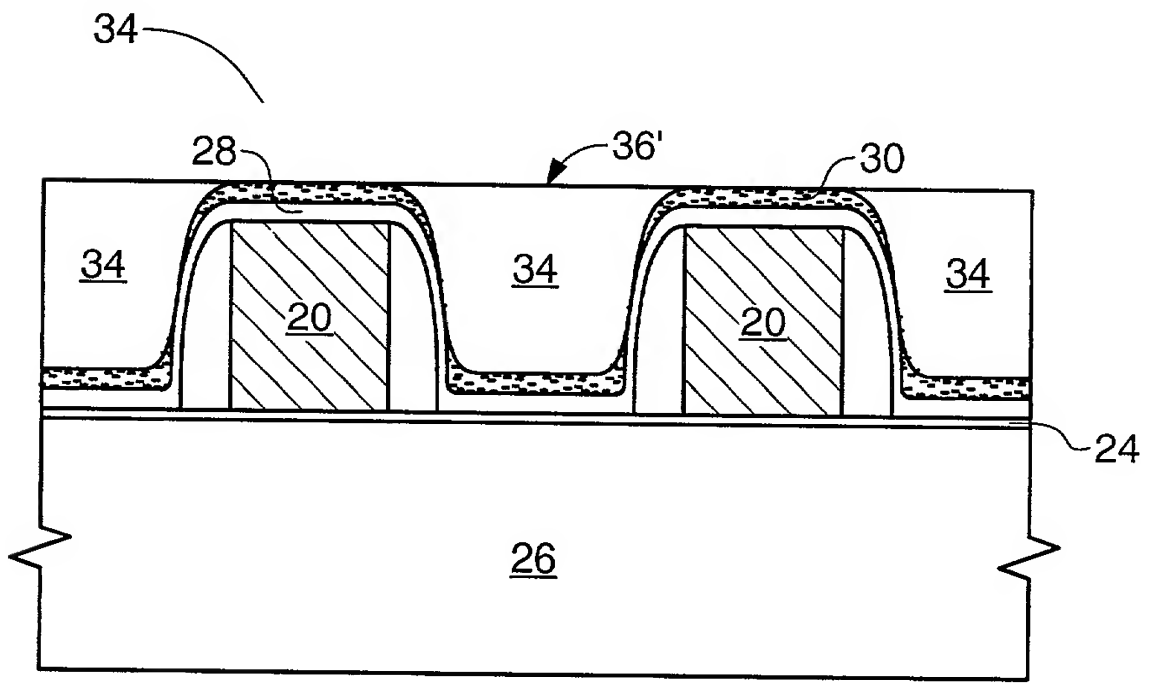

FIG. 6

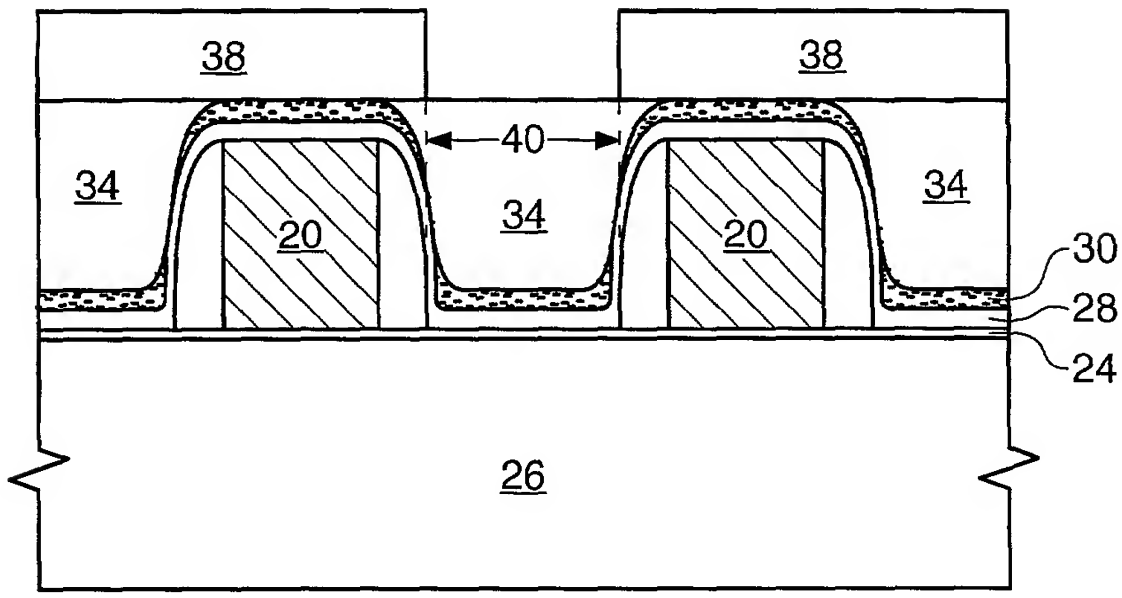

FIG. 7

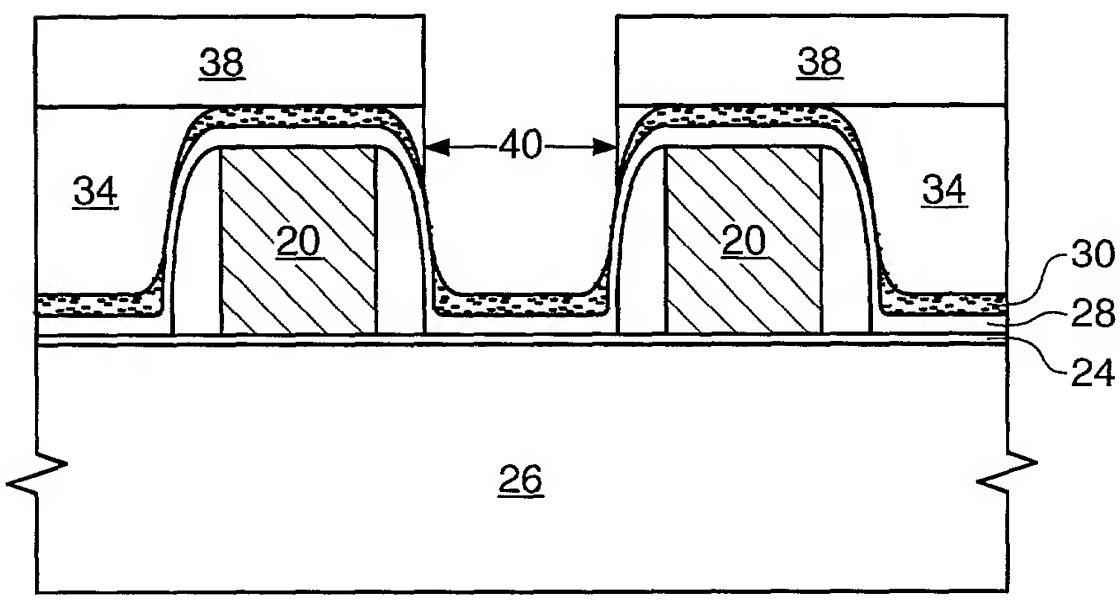

FIG. 8

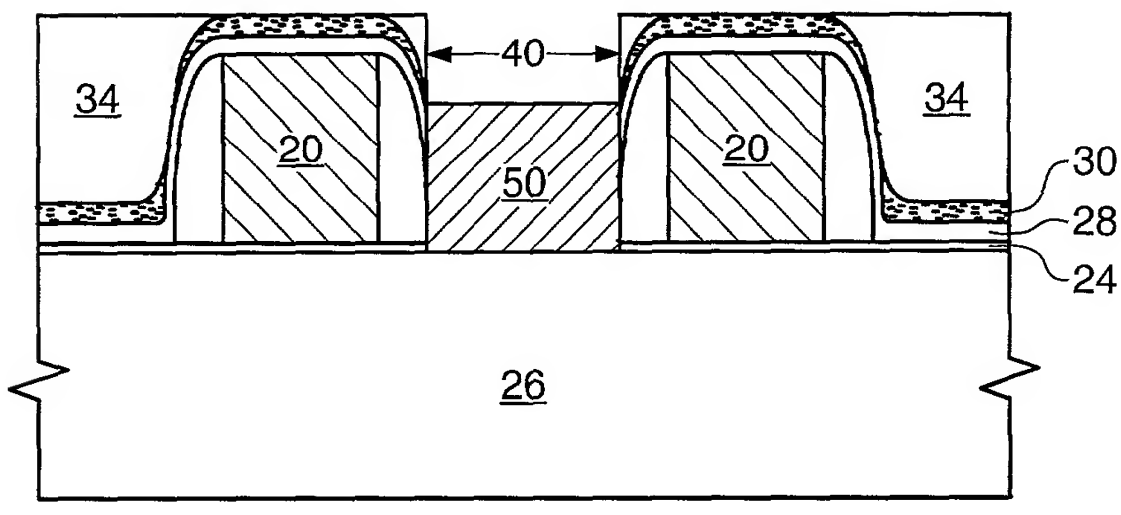

FIG. 9

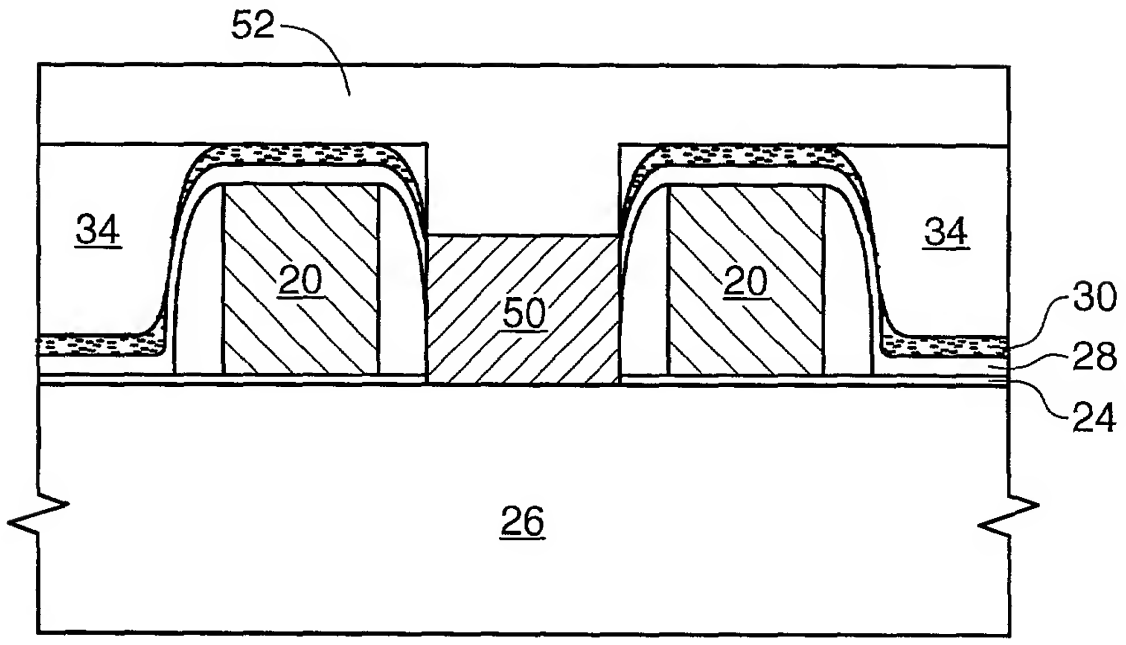

FIG. 10

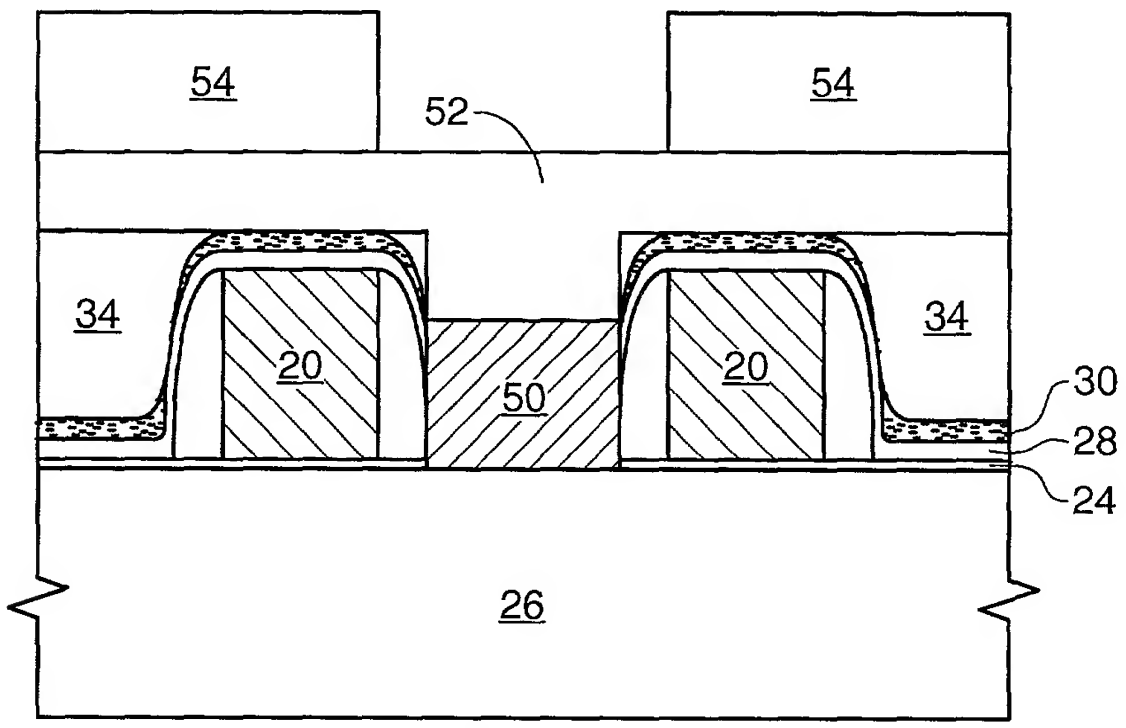

FIG. 11

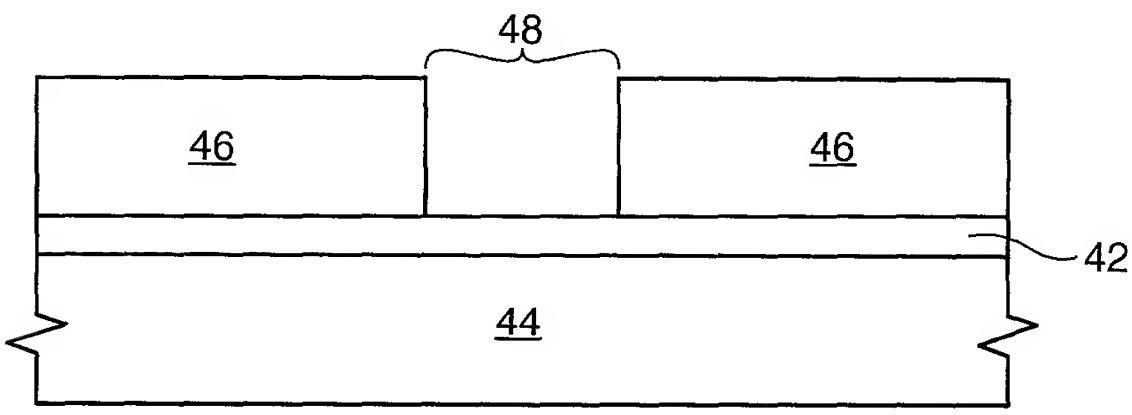

FIG. 12

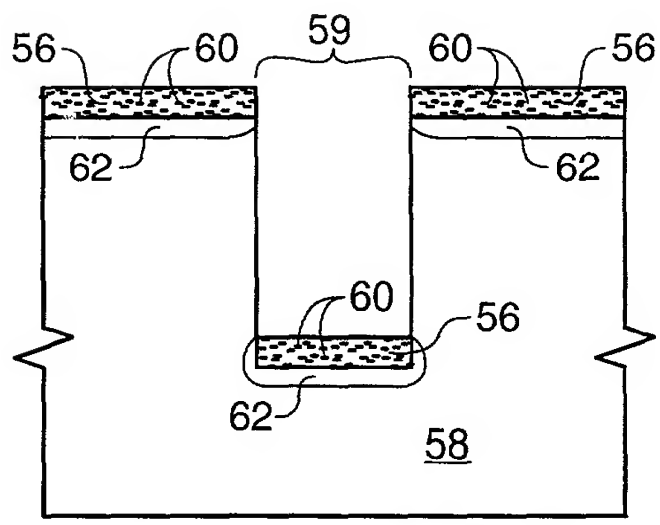

FIG. 13

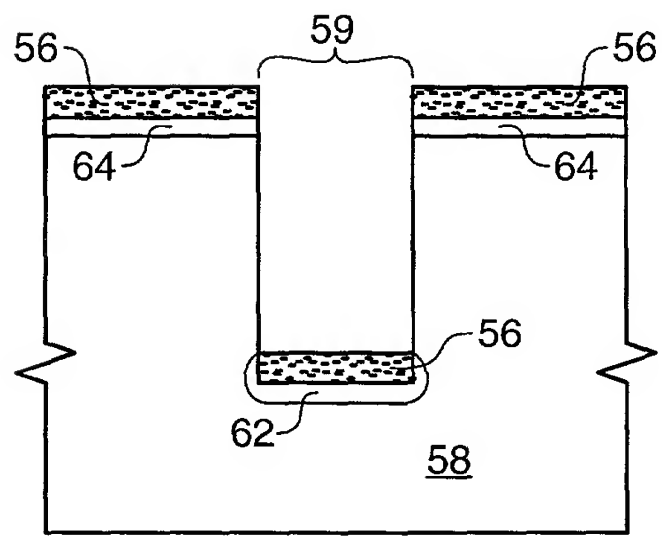

FIG. 14

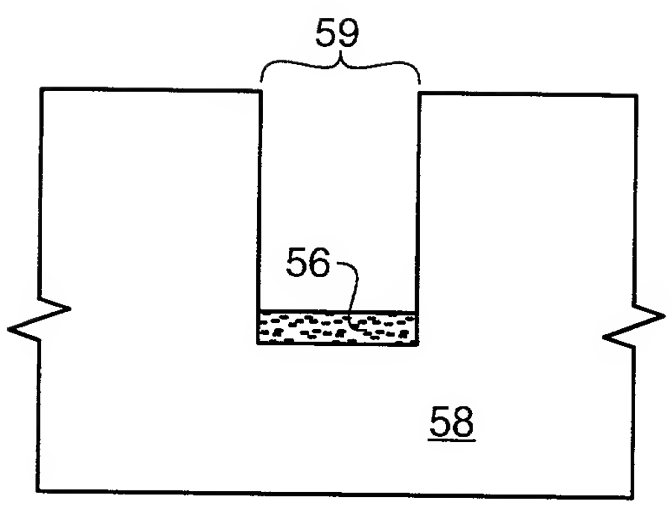

FIG. 15

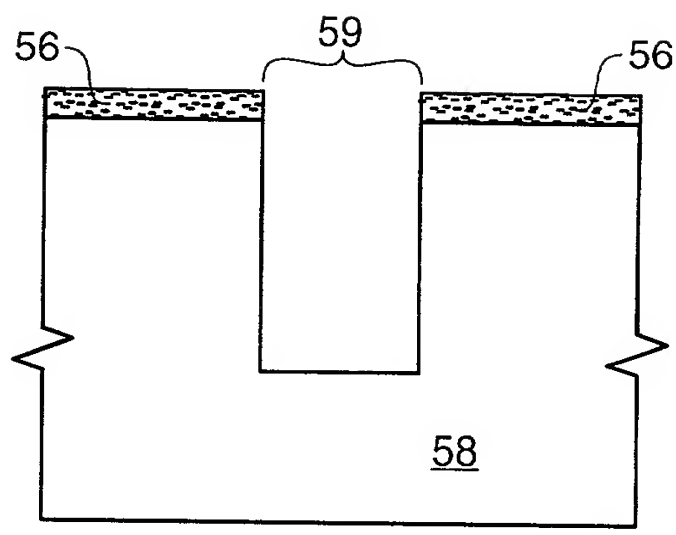

FIG. 16

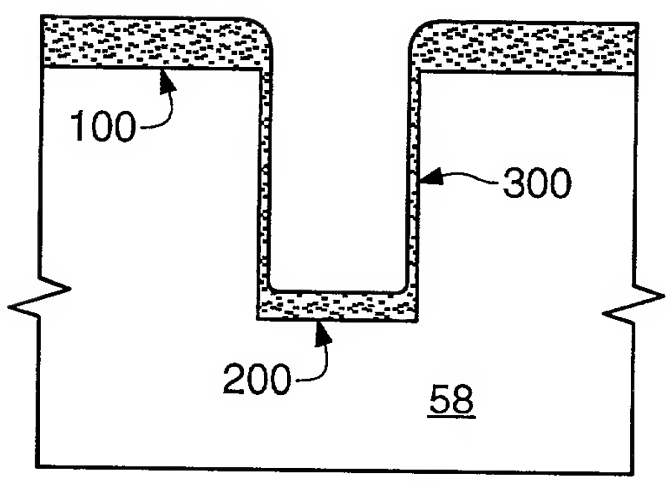

FIG. 17

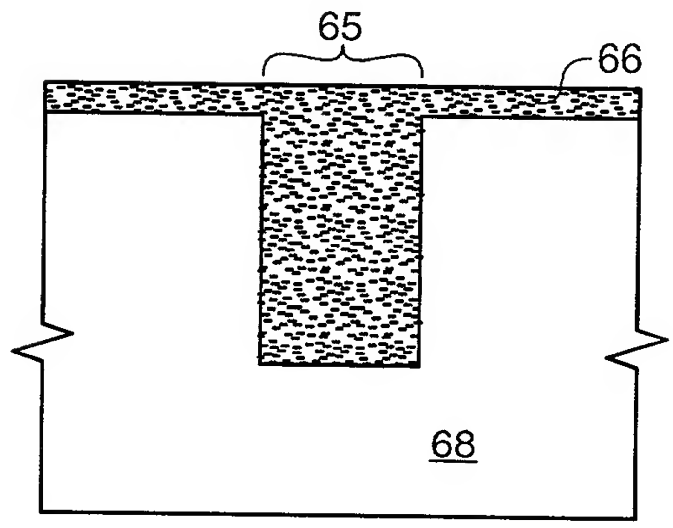

FIG. 18

DOCKET NO.: 98-01191.01

SUBSTITUTE SPECIFICATION
(CLEAN VERSION)

FOR

METHOD TO FORM ETCH AND/OR CMP STOP LAYERS

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A METHOD TO FORM ETCH AND/OR CMP STOP LAYERS

Related Application

[0001] This application is a divisional of application serial number 09/531,680, filed March 20, 2000.

Technical Field

[0002] The present invention relates generally to a doped non-conformal layer in a semiconductor device. More specifically, the present invention relates to a boron-doped oxide that can be used as a stopping layer for etching or chemical-mechanical planarization (CMP), among other uses.

Background of the Invention

[0001] The formation of semiconductor devices (which may actually include conductive and insulative materials as well as semiconductive elements) often involves removing amounts of material included as part of the device. Occasionally, the desired result of removing material is a planarized surface. Other times, the desired result is an opening extending at least partway into the material. Examples of both results occur in the manufacture of dynamic random access memory (DRAM) devices, wherein transistor gates are formed over a semiconductor substrate. Once the gates are formed, an insulator can be deposited between and over them. The surface of this insulator is lowered to the general level of the gate top and planarized through etching or CMP. After that, a contact opening is etched through the insulator to a doped region of the semiconductor substrate that forms a transistor source or drain. This opening will subsequently be filled with conductive material, thereby allowing electrical communication with the doped substrate.

[0002] This process of forming a hole within an insulation layer and filling that hole with a conductive material is generally known as a damascene process. Damascene processes offer an alternative to etching away undesired portions of a continuous conductive layer and surrounding the remaining portions with insulation. Damascene processes used at various fabrication stages provide additional examples of where material removal is desired in the context of DRAM devices. For example, initially providing the damascene insulation layer may involve CMP before the hole is formed therein, and forming the hole usually involves an etching step.

[0003] During CMP or etching steps such as those described above, it is often preferable to provide some sort of CMP stop or etch stop at a location defining the extent of the removal process. Oftentimes this CMP/etch stop will be some sort of material that is more resistant if not completely immune to the CMP/etch process than is the material that is to be removed. For example, United States Patent 5,485,035 by Lin et al. discloses using a first boron-doped oxide layer in carrying out a planarizing etch back (see Lin's Fig. 3) and a second boron-doped oxide layer to stop the via etch through an overlying insulating layer (Lin's Fig. 5).

[0004] Such oxides can be deposited by growing them from a surface in an oxidizing atmosphere or by conventional deposition methods, such as chemical vapor deposition (CVD). Another method of providing oxide is a process known as Flowfill. Flowfill involves reacting silane with vaporized hydrogen peroxide. The reaction results in a gas which condenses as a liquid on a substrate cooled to about 0°C. A subsequent heat treatment dries the liquid to form SiO_2.

[0005] As for the application of Flowfill-created oxides, prior art discloses a CMP process that stops within a Flowfill layer, although it is unclear from one particular reference whether this is a matter of properly timing the CMP or due to some property of the oxide itself. *See* Sabine Penka, *Integration Aspects of Flowfill and Spin-on-Glass Process for Sub-0.35μm Interconnects*, PROCEEDINGS OF THE IEEE 1998

INTERNATIONAL INTERCONNECT TECHNOLOGY CONFERENCE, at 271 (1998). Significantly, this reference further specifies that "Flowfill . . . need[s] to be enclosed by a base and a cap oxide." Other references further emphasize the presence of a base and cap. See, e.g., U. Höckele, et al., *Flowfill-Process as a New Concept for Inter-Metal-Dielectrics*, MATERIALS SCIENCE FORUM, at 235 (1998); A. Hass Bar-Ilan et al., *A comparative study of sub-micron gap filling and planarization techniques*, PROCEEDINGS OF THE SPIE – THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING, at 278-279 (1995); K. Beekmann et al., *SUB-MICRON GAP FILL AND IN-SITU PLANARISATION USING FLOWFILL™ TECHNOLOGY*, at 137 (1996). The base layer is an oxide provided by plasma-enhanced CVD (PECVD) and serves as an adhesion layer for the Flowfill oxide.

[0006] Concerning altering the properties of Flowfill layers, U.S. Pat. No. 5,985,770, also assigned to Micron Technology Inc., discloses gas phase doping of a Flowfill layer before or during the heat treatment that ultimately solidifies the Flowfill liquid into SiO_2.

[0007] Given the state of the prior art in terms of CMP and etch stops, there is a constant need in the art to find a new etch stop or CMP stop and new ways of making them. Moreover, there is also a need in the art to find new applications for and modifications of the Flowfill process.

Summary of the Invention

[0008] Accordingly, exemplary embodiments of the current invention provide a doped non-conformal oxide. In a preferred exemplary embodiment, a non-conformal oxide that resists doping is initially provided by way of a Flowfill process. Next is provided a second non-conformal oxide that is configured to accept dopant more readily. Subsequently the second oxide is annealed in an atmosphere containing boron. Alternative method embodiments include other ways of flowing at least one of

the oxides. Still other alternatives address other ways of providing non-conformal oxides, such as through a high-density plasma CVD. Yet other alternative exemplary embodiments address the use of a doped non-conformal oxide as an etch stop and/or a CMP stop.

Brief Description of the Drawings

[0009] FIG. 1 depicts a cross section of an in-process DRAM as known in the prior art.

[0010] FIGS. 2-11 illustrate cross-sections of an in-process DRAM having undergone steps in exemplary method embodiments of the current invention. These figures also show various exemplary apparatus embodiments within the scope of the current invention.

[0011] FIG. 12 illustrates a modified damascene process included as an exemplary embodiment of the current invention.

[0012] FIG. 13 shows a cross-section of an in-process semiconductor device portion having undergone steps included in another exemplary embodiment of the current invention.

[0013] FIG. 14 shows a cross-section of an in-process semiconductor device portion having undergone steps included in an alternative exemplary embodiment of the current invention.

[0014] FIG. 15 is a cross-section of an exemplary apparatus embodiment of the current invention.

[0015] FIG. 16 is a cross-section of another exemplary apparatus embodiment of the current invention.

[0016] FIG. 17 is a cross-section of still another exemplary apparatus embodiment of the current invention.

[0017] FIG. 18 shows a cross-section of an in-process semiconductor device portion having undergone steps included in yet another exemplary embodiment of the current invention.

Detailed Description of the Preferred Embodiment

[0018] FIG. 1 depicts a portion of a wafer in the process of having DRAM devices formed thereon. Specifically, FIG. 1 shows two transistor gates 20 flanked by insulating spacers 22. The gates 20 may include one or more conductive layers and an insulating cap. Further, the transistor gates 20 are over a gate oxide 24 which, in turn, overlies a substrate 26. In the current application, the term "substrate" or "semiconductor substrate" will be understood to mean any construction comprising semiconductor material, including but not limited to bulk semiconductive materials such as a semiconductor wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). Further, the term "substrate" also refers to any supporting structure including, but not limited to, the semiconductive substrates described above.

[0019] FIG. 2 illustrates a step taken as part of an exemplary method embodiment of the current invention. A first oxide 28 is provided over the transistor gates. Preferably the first oxide 28 is provided by the Flowfill process mentioned above. More specifically, the first oxide 28 is provided by reacting silane (SiH_4) with hydrogen peroxide (H_2O_2) at a pressure of about 1 Torr, a substrate temperature of 0°C, an SiH_4 flow rate of about 100 sccm, and an H_2O_2 flow rate of about 0.6g/minute. The result is silanol ($Si(OH)_4$) – a liquid that flows over the cooled substrate. Once deposited, heating the liquid $Si(OH)_4$ to about 450°C forms solid

SiO_2. As a result of this process, the first oxide 28 not only deposits on top of the gates 20 but also between them. However, the first oxide 28 is non-conformal in that horizontal portions are thicker than non-horizontal portions. Of further note is that this Flowfill process is used without necessarily providing an adhesion layer. In addition, the use of SiH_4 results in an oxide that will not readily accept dopant.

[0020] FIG. 3 illustrates that a second oxide 30 is subsequently deposited over the first oxide 28. Preferably, deposition occurs *in situ* -- in the same chamber as the previous oxide deposition. For this second oxide 30, it is preferred to react methylsilane -- H_3SiCH_3 -- with hydrogen peroxide -- H_2O_2 -- under parameters similar to those described above. The result is a flowable material (plus organic by products). This material can be considered an oxide precursor in that it forms SiO_2 after being heated to about 450°C. Accordingly, such a thermal treatment is carried out, thereby forming the second oxide 30. Like the first oxide 28, second oxide 30 deposits non-conformally with respect to the underlying surface. For example, in the exemplary embodiment pictured, the thickness of the second oxide 30 over a particular horizontal surface is generally constant given the self-planarizing nature of the deposition. Regarding non-horizontal surfaces, the second oxide 30 will vary in thickness and, in fact, may not deposit at all on some non-horizontal surfaces. Acceptable exemplary thicknesses for the second oxide 30 in this embodiment include 500 to 1000 Angstrom-thick horizontal portions and 0-50 Angstrom-thick non-horizontal portions. Thus, in at least some embodiments, the location of the second oxide 30 is limited to discrete portions of the underlying support structure or structures.

[0021] Unlike the first oxide 28, this second oxide 30 is porous and will readily accept dopant. Without limiting the current invention, it is believed that this second oxide 30 will do so because of its porous nature. As for the creation of these pores, it is thought that the formation process described above results in gaps within the second oxide 30 that are bigger than the lattice constant defined by the Si-O bonds of

that layer. These gaps, which may define lengths of 10 to 20 Angstroms and greater, may accommodate a dopant that is supplied in a later step. Accordingly, the term "pore" as used in this application, including the claims, is defined as a gap in a material, wherein the gap is bigger than the lattice constant of that material.

[0022] Accordingly, the second oxide 30 is subsequently doped with boron 32, the result of which is seen in FIG. 4. One way of doping is to anneal the second oxide 30 in an atmosphere containing boron. Exemplary parameters for such an anneal include an atmosphere wherein diborane (B_2H_6) contributes at least a partial pressure of the ambient; a temperature of 400-800°C; a pressure ranging from 0.5 Torr to 760 Torr; and a process time ranging from 10 seconds to 5 minutes. The first oxide layer 28 prevents most if not all diffusion of boron into other portions of the in-process DRAM device.

[0023] Next, an insulation layer 34 seen in FIG. 5 is layered over the in-process DRAM. This insulation layer is preferably formed of a glass such as borophosphosilicate glass (BPSG). The deposition of BPSG is a somewhat conformal process, resulting in an insulation layer 34 having a non-planarized surface 36. To achieve the desired planarized surface for that layer 34, a CMP process known in the art may be enacted. The portions of second oxide 30 atop the transistor gates 20, being harder to planarize than the overlying insulation layer 34, act as a CMP stop layer. The result, seen in FIG. 6, is an insulation layer 34 having a planarized surface 36' at the level defined by the second oxide 30 atop the gates 20.

[0024] Moreover, the lower portions of the second oxide 30 may also serve to stop another removal process. For example, it may be desired to provide a contact between the transistor gates 20. To do so, FIG. 7 illustrates that a layer of photoresist 38 is deposited over insulation layer 34 and patterned to expose a contact site 40. A subsequent etching step removes the insulation layer 34 material from contact site 40 yet has greater difficulty in removing the second oxide 30 near the bottom of the

contact site 40, as seen in FIG. 8. As an example, the in-process device can be exposed to a low-pressure HF vapor or a buffered HF solution at 23°C, which will etch BPSG to a greater degree than the boron-doped second oxide 30. The second oxide 30 may then be removed by a second etch. This second etch may take place in the form of another wet etch using HF. Alternatively, a reactive sputter etch or a plasma etch may be performed using gases such as CHF_3, CF_4, and C_2F_6. Exemplary plasma etch parameters include using CF_4 at a flow rate of 50 sccm, CHF_3 at a flow rate of 50 sccm, argon at a flow rate of 1000 sccm, a chamber pressure ranging from 0.2 to 0.002 torr, and an RF power of 750 W, for a time necessary to sufficiently remove enough of the second oxide 30. This etch may be used to remove the first oxide 28 and gate oxide 24 as well. Alternatively, separate etch steps may be applied to these oxides. Subsequent processing steps known in the art may be carried out to complete the DRAM.

[0025] The subsequent processing steps, however, may lead to other exemplary embodiments involving a non-conformal boron-doped oxide. FIG. 9 illustrates that a polycrystalline plug 50 is eventually deposited within the contact site 40. Assuming the in-process DRAM device will be incorporating capacitors using high-K dielectrics, it will be preferred to recess the plug 50 so that its surface does not reach the top of the contact site 40. As shown in FIG. 10, a non-conformal insulator 52, which can be formed in a manner such as that used to form the second oxide 30 above, may be deposited and doped with boron. Thereafter, a damascene process may be used to define a container in which a capacitor will appear. For example, a layer of insulation 54 as shown in FIG. 11 can be deposited and etched according to a patterned mask (not shown), with the non-conformal insulator 52 used to stop that etch. An additional etch may then be used to clear the boron-doped non-conformal insulator 52 from above the plug 50. However, this etch is optional. Regardless of whether this optional etch is performed, processing may continue, including steps that provide a capacitor within the container.

[0026] FIG. 12 demonstrates that non-conformal etch stops apply to other damascene-created structures as well. In that figure, an oxide layer 42 has been deposited over a support surface 44 (assumed to be a BPSG layer) and subsequently annealed in a boron-containing atmosphere. An insulating layer 46 is then deposited thereover and patterned according to a mask (not shown) to form an opening 48 configured to receive a conductive material. The etch process used to form the opening 48 will generally stop once the oxide layer 42 is reached.

[0027] The current invention also includes within its scope exemplary embodiments wherein the doped non-conformal oxide is used for purposes other than stopping etching or CMP. In FIG. 13, for example, a non-conformal oxide 56 has been deposited onto the surface of a material 58 and at the bottom of a trench 59 defined by that material 58. The material 58 is assumed to be BPSG but could be another material. Annealing the non-conformal oxide 56 in diborane using the parameters discussed above implants boron 60 into the non-conformal oxide 56. Further annealing of that oxide 56 can drive the boron 60 into adjacent regions 62 of the material 58. The non-conformal oxide 56 may then be removed, leaving a trench 59 having a doped bottom and substantially undoped sides, and the material 58 around the trench 59 having a doped surface.

[0028] Alternatively, if it is not desired to dope the surface of material 58, a barrier layer 64 such as a nitride may be deposited before etching the trench 59. The result after annealing the boron-doped non-conformal oxide 56 is depicted in FIG. 14. Yet another alternative is to remove the doped surface by way of a planarization step, such as CMP, performed before annealing.

[0029] Still another alternative is to provide process parameters such that the deposition of the non-conformal oxide on the top of the material 58 is reduced or perhaps even eliminated. For example, if methylsilane is reacted with hydrogen peroxide at room temperature (about 20°C), then the non-conformal oxide 56 will be

thicker at the bottom of trench 59 than amounts, if any, at the top, as seen in FIG. 15. Further, it is also believed that, as the temperature during deposition approaches 100°C, the non-conformal oxide will deposit a thicker amount on the surface than at the bottom of a trench 59 in that surface, an extreme result of such being depicted in FIG. 16. Thus, as seen in FIG. 17, the current invention includes within its scope exemplary embodiments wherein a non-conformal doped oxide has different thicknesses on a first horizontal surface 100, a second horizontal surface 200, and a non-horizontal surface 300 of a device, wherein such thicknesses are determined by process parameters including the ones addressed above. Further, the thickness at any of these regions may be reduced to zero.

[0030] In other cases, it may simply be desired to fill a trench 65 with a doped oxide, and embodiments of the current invention can accommodate such cases. A non-conformal oxide 66 can be deposited and subsequently doped, using, for example, the methylsilane deposition/diborane anneal steps discussed above. The result is seen in FIG. 18. The oxide 66 can be subsequently etched or CMP'd to make the oxide 66 generally level with the surface of support material 68. Currently, borosilicate glass (BSG) is deposited in such trenches by way of conventional means, but as trenches become narrower in width, standard BSG deposition methods may not work. Thus, this exemplary embodiment offers an alternative method for filling trenches with a boron-doped insulator. In fact, the boron-doped insulator in this and other exemplary embodiments could be considered to be a low dielectric constant (low-K) BSG, wherein a low dielectric constant is considered to be at most 3. Accordingly, exemplary embodiments of the current invention have applications in other contexts where BSG or other low-K dielectrics are used. For example, a doped non-conformal oxide could be used as an interlayer dielectric (ILD).

[0031] In addition, while it is preferred to deposit the oxide by heating the product of a methylsilane/hydrogen peroxide reaction, the current invention includes within its scope exemplary embodiments that provide a non-conformal oxide by other ways.

For example, another way to flow the oxide onto the underlying layer is through a spin-on-glass (SOG) process. The SOG process involves depositing a suspension of glass particles in an inorganic carrier onto a spinning substrate. Conventional photoresist tools can be used to achieve such a deposition. The organic carrier is then driven off of the substrate using a thermal process, and the remaining glass is reflowed to fill spaces in the underlying topography and to planarize the glass surface.

[0032] Another way of providing a non-conformal oxide is through the use of a high-density plasma (HDP) CVD process. In such a process, plasma gases including silicon-containing, oxygen-containing, and nonreactive gasses (e.g. a noble gas) are used to deposit an oxide while simultaneously etching the oxide to prevent gaps from forming in the oxide material. The density of the plasma is greater than 10^{10} ions per cm^3. Exemplary parameters include an ambient of O_2 (flowed at a rate of 120-500 sccm), SiH_4 (flowed at a rate of 80-250 sccm), and Ar (flowed at a rate of 0-50 sccm); an RF bias at 13.56 MHz; a temperature ranging from 350-700°C; and a bias power ranging from 0 to 2000 W. Moreover, other CVD processes could be used to provide a non-conformal layer.

[0033] In addition, it is not necessary that the dopant be boron. Exemplary embodiments of the current invention include those in which at least one other impurity replaces or is added along with boron. It is noted that U.S. Pat. No. 5,985,770 discussed above discloses doping the oxide precursor with various materials before and during formation of the oxide layer. For example, application '987 indicates that phosphorous doping can be accomplished using PH_3, phosphates, or phosphites; fluorine doping can involve NF_3 or F_2; carbon may serve as the dopant using C_2H_6, trimethyl silane ($(CH_3)_3SiH$) or CH_4; and nitrogen may dope the oxide using NF_3 or NH_3. The current invention includes within its scope exemplary embodiments that involve doping a non-conformal oxide after its formation with the dopants above (either alone or in combination) by using precursor gases such as the ones above (again either alone or in combination). More specific exemplary

embodiments include doping one portion of the non-conformal oxide with a first dopant and a second portion of the oxide with a second dopant. Appropriate masking of the portions can be used to allow for such selective doping.

[0034] Furthermore, in embodiments wherein a diffusion barrier layer (such as the first oxide 28) is preferred, it is not necessary that the diffusion barrier be deposited in a non-conformal manner. Other exemplary embodiments allow for the barrier layer to be provided through standard methods resulting in a conformal layer. For example, an SiO_2 barrier layer could be provided under known conformal CVD parameters. Alternatively, a conformal layer of tetraethylorthosilicate (TEOS)-based glass could be layered before the non-conformal layer is provided and subsequently doped.

[0035] Given the variety of alternative embodiments described above, one skilled in the art can appreciate that, although specific embodiments of this invention have been described above for purposes of illustration, various modifications may be made without departing from the spirit and scope of the invention. Returning to the first exemplary embodiment described above, for instance, the first oxide under the doped second oxide is preferred to help prevent diffusion into other portions of the DRAM. However, the first oxide is not required, as careful processing can dope the second oxide without having the dopant diffuse beyond the oxide. Thus, embodiments without the first oxide fall within the scope of the invention. Further, as an addition to or an alternative to the preferred monomethylsilane/peroxide reaction, the current invention includes within its scope the use of other chemicals to provide a non-conformal oxide, including (but not limited to) dimethylsilane, trimethylsilane, tetramethylsilane, pentamethyldisilane, and combinations of chemicals. Moreover, while exemplary embodiments of the current invention have been illustrated in the context of a DRAM, these and other embodiments apply to semiconductor devices in general. Accordingly, the invention is not limited except as stated in the claims.

Claims

What is claimed is:

1. A memory device, comprising:

a circuit device defining a horizontal surface and a non-horizontal surface; and

a porous oxide over said circuit device, said porous oxide having a first thickness extending perpendicularly from said horizontal surface and a second thickness extending generally perpendicularly from said non-horizontal surface, wherein said second thickness is different from said first thickness.

2. The memory device in claim 1, wherein said porous oxide comprises an oxide defining at least one pore.

3. The memory device in claim 2, wherein said porous oxide comprises a plurality of silicon atoms and a plurality of oxygen atoms, wherein said plurality of silicon atoms and said plurality of oxygen atoms define a lattice constant; and wherein at least one dimension of said at least one pore is greater than said lattice constant.

4. The memory device in claim 3, wherein said dimension of said at least one pore is at least 10 angstroms.

5. The memory device in claim 4, wherein said dimension of said at least one pore ranges from 10 to 20 angstroms.

6. The memory device in claim 4, further comprising a dopant in at least one pore.

7. The memory device in claim 6, wherein said dopant consists of a selection from boron, carbon, phosphorous, fluorine, nitrogen, and combinations thereof.

8. A portion of a semiconductor device, comprising:

a support surface defining at least two elevations within said semiconductor device; and

a doped insulator non-conformally over said support surface, wherein said insulator is thinner between two consecutive elevations of said support surface than said insulator directly over at least one of said consecutive elevations.

9. The portion of a semiconductor device in claim 8, wherein said doped insulator is non-continuously over said support surface.

10. The portion of a semiconductor device in claim 8, wherein said doped insulator is a boron-doped insulator.

11. The portion of a semiconductor device in claim 8, wherein said doped insulator is a doped oxide.

12. The portion of a semiconductor device in claim 8, further comprising an undoped insulator between said doped insulator and said support surface.

13. The portion of a semiconductor device in claim 12, wherein said undoped insulator is non-conformally over said support surface.

14. A material for a semiconductor device, comprising a boron-doped oxide on at least one horizontal portion of said semiconductor device more so than on a vertical portion of said device.

15. The material in claim 14, wherein said semiconductor device includes a layer defining a trench; wherein said at least one horizontal portion comprises a bottom of said trench; and wherein said vertical portion is a sidewall of said trench.

16. The material in claim 15, wherein said at least one horizontal portion further comprises a surface of said layer even with a top of said trench.

17. A method of processing an in-process semiconductor device, comprising:

non-conformally depositing an oxide over said in-process semiconductor device;

doping said oxide; and

depositing an insulator over said oxide.

18. The method in claim 17, further comprising:

initiating a removal of at least a portion of said insulator; and

halting said removal using said oxide.

19. The method in claim 18, wherein said initiating step comprises initiating an etching of said insulator; and wherein said halting step comprises using said oxide as an etch stop.

20. The method in claim 18, wherein said initiating step comprises initiating a planarization of said insulator.

21. The method in claim 20, wherein said step of initiating a planarization of said insulator comprises initiating a chemical-mechanical planarization of said insulator; and wherein said halting step comprises using said oxide as a CMP stop.

22. A method of providing oxide for an in-process semiconductor device, comprising:

depositing a first oxide over said in-process semiconductor device; and

non-conformally depositing a porous second oxide onto said first oxide.

23. The method in claim 22, wherein said step of depositing a first oxide comprises depositing said first oxide in a chamber; and wherein said step of non-conformally

depositing a porous second oxide comprises depositing said second oxide in said chamber.

24. The method in claim 22, wherein said step of non-conformally depositing a porous second oxide comprises reacting methylsilane with hydrogen peroxide.

25. The method in claim 22, wherein said step of non-conformally depositing a porous second oxide comprises reacting H_3SiCH_3 with H_2O_2.

26. The method in claim 25, wherein said step of non-conformally depositing a porous second oxide further comprises:

cooling said in-process semiconductor device to about 0°C before said reacting step; and

providing a temperature of about 450°C inside said chamber after said reacting step.

27. The method in claim 26, wherein said step of depositing a first oxide comprises reacting silane with hydrogen peroxide.

28. A method of providing a doped oxide, comprising:

flowing an oxide precursor over a portion of a semiconductor device;

forming an oxide from said precursor; and

subsequently annealing said oxide in an atmosphere containing a dopant.

29. The method in claim 28, wherein said annealing step comprises annealing said oxide in an atmosphere consisting of a selection of PH_3, a phosphate, a phosphite, NF_3, F_2, C_2H_6, trimethyl silane, CH_4, NH_3, B_2H_6, and combinations thereof.

30. The method in claim 29, wherein said annealing step further comprises annealing at a temperature ranging from 400 to 800°C, at a pressure ranging from 0.5 to 760 Torr, and for a time ranging from 10 seconds to 5 minutes.

31. A method of processing a surface of an in-process memory device, comprising:

providing said surface as part of said memory device using a non-CVD process;

flowing a material onto said surface;

turning said material into a first oxide; and

doping said first oxide.

32. The method in claim 31, wherein said step of providing said surface comprises providing a barrier oxide using a Flowfill process; and wherein said method further comprises blocking diffusion of a dopant from said first oxide using said barrier oxide.

33. The method in claim 32, wherein said step of doping said first oxide comprises:

doping a first portion of said first oxide with a first impurity; and

doping a second portion of said first oxide with a second impurity.

34. A method of providing an etch stop for a semiconductor device, comprising:

providing at least one support surface as part of said semiconductor device, said surface having a horizontal portion and a non-horizontal portion;

depositing an oxide onto said support surface, wherein said oxide has a uniform thickness on said horizontal portion and a variable thickness on said non-horizontal portion; and

doping said oxide.

35. The method in claim 34, wherein said depositing step comprises depositing said oxide by way of a CVD process.

36. The method in claim 35, wherein said depositing step comprises depositing said oxide by way of an HDP CVD process.

37. A method of providing a CMP stop for a semiconductor device, comprising:

providing an element of said semiconductor device, said element having a top and a side;

depositing an oxide over said element, wherein said depositing leaves more of said oxide on said top than on said side; and

annealing said oxide in a doping atmosphere.

38. The method in claim 37, wherein said step of depositing an oxide comprises:

flowing a precursor to said oxide over said element; and

heating said precursor.

39. The method of claim 38, wherein said step of depositing an oxide comprises depositing said oxide using a spin-on-glass process.

40. A method of selectively doping a circuit device material, comprising:

depositing an oxide over a first horizontal surface of said circuit device material to the exclusion of a vertical surface of said material;

introducing a dopant into said oxide; and

diffusing said dopant from said oxide into said material.

41. The method in claim 40, further comprising a step of depositing a diffusion barrier over a second horizontal surface of said material; and wherein said step of depositing an oxide further comprises depositing said oxide over said diffusion barrier.

42. A method of filling a trench included as part of a semiconductor device, comprising:

reacting methylsilane with hydrogen peroxide in a chamber containing said semiconductor device;

allowing a product from a reaction of said methylsilane and said hydrogen peroxide to at least fill said trench;

changing said product into a silicon oxide; and

heating said silicon oxide in a boron atmosphere.

43. A fabrication process for a DRAM including a semiconductor substrate, said process comprising:

depositing an undoped self-planarizing first oxide over an in-process device included as a part of said DRAM;

depositing an undoped self-planarizing second oxide over said first oxide; and

doping said second oxide.

44. The process in claim 43, further comprising:

depositing an insulation layer over said second oxide;

planarizing said insulation layer; and

using said second oxide as a planarization stop.

45. The process in claim 43, further comprising:

depositing an insulation layer over said second oxide;

etching an opening in said insulation layer; and

using said second oxide as an etch stop.

46. The process in claim 45, wherein said step of using said second oxide as an etch stop comprises using a portion of said second oxide over said substrate as said etch stop.

47. The process in claim 46, said step of etching an opening in said insulation layer comprises etching said insulation layer at a first etch rate; and wherein said step of using said second oxide as an etch stop comprises etching said second oxide at a second etch rate, wherein said second etch rate is less than said first etch rate.

48. The process in claim 47, wherein said step of etching said insulation layer comprises exposing said insulation to a selection of an HF vapor and an HF liquid.

49. The process in claim 48, wherein said step of etching said insulation layer comprises exposing said insulation to a buffered HF liquid having a temperature of about 23°C.

50. The process in claim 48, wherein said step of etching said second oxide comprises exposing said second oxide to said selection.

51. A damascene process, comprising:

providing a material over a semiconductor substrate, said material having a fluid property;

forming an oxide from said material in response to allowing said material to lose said fluid property;

providing an insulation layer over said oxide;

etching an opening in said insulation layer;

halting said etching with said oxide; and

depositing a conductive material within said opening.

52. The damascene process in claim 51, further comprising a step of removing at least a portion of said oxide after said halting step and before said depositing step.

53. The damascene process in claim 52, wherein said step of forming an oxide comprises:

forming said oxide onto a BPSG layer; and

doping said oxide before said step of providing an insulation layer.

54. The damascene process in claim 52, wherein:

said step of providing a material comprises depositing said material having a planar surface and defining at least two different thicknesses, wherein depositing said material occurs before providing said insulation layer; and

said method further comprises doping said oxide before providing said insulation layer.

55. The damascene process in 54, wherein said step of depositing said material comprises depositing said material over a gate and over a conductive plug next to said gate, wherein a top of said plug is lower in elevation than a top of said gate.

56. The damascene process in claim 55, wherein said etching step comprises etching using a selection of a reactive sputter process and a plasma process.

57. The damascene process in claim 56, wherein said etching step comprises plasma etching using a gas comprising fluorine, wherein said gas includes a selection of CHF_3, CF_4, and C_2F_6.

58. The damascene process in claim 57, wherein said plasma etching step comprises:

providing a chamber configured to accommodate said semiconductor substrate;

flowing CF_4 into said chamber at a rate of 50 sccm;

flowing CHF_3 into said chamber at a rate of 50 sccm;

flowing Argon into said chamber at a rate of 1000 sccm;

providing pressure of 0.2 to 0.002 Torr inside said chamber; and

providing 750 W of RF power to said chamber.

59. A method of forming oxide over a transistor gate and over a substrate extending laterally from under said gate, said method comprising:

forming an undoped first oxide over said gate and said substrate;

forming an undoped second oxide over said first oxide;

doping said second oxide after forming said second oxide;

depositing insulation over said second oxide after doping said second oxide;

initiating a removal of a portion of said insulation; and

stopping said removal with said second oxide.

60. The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a TEOS-based oxide.

61. The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a continuous silicon dioxide layer.

62. The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a first oxide that is thicker over said gate than lateral to said gate, and wherein said first oxide is thicker over said substrate than lateral to said gate.

63. The method in claim 62, wherein said step of forming an undoped first oxide comprises forming a non-porous first oxide.

64. The method in claim 62, wherein said step of forming an undoped second oxide comprises forming a second oxide that is thicker over said gate than lateral to said gate, and wherein said second oxide is thicker over said substrate than lateral to said gate.

65. The method of claim 64, wherein said step of forming an undoped second oxide comprises:

depositing 500 to 1000 Angstroms of said second oxide over said gate;

depositing 500 to 1000 Angstroms of said second oxide over said substrate; and

depositing 0 to 50 Angstroms of said second oxide lateral to said gate.

66. A method of depositing an interlayer dielectric, comprising:

providing a first level of a semiconductor device, said first level defining a topography and comprising insulation;

depositing BSG onto discrete portions of said topography, said BSG having a dielectric constant of at most 3; and

providing a second level of said semiconductor device over said BSG.

67. The method in claim 66, wherein said step of depositing BSG comprises:

depositing glass onto said topography, said depositing resulting in a planar surface of said glass; and

lowering a dielectric constant of said glass.

68. The method in claim 67, wherein said step of depositing glass comprises:

flowing a silicon oxide precursor over said topography; and

hardening said precursor into a silicon oxide.

69. The method in claim 68, wherein said step of lowering a dielectric constant of said glass comprises doping said silicon oxide with boron.

70. The method in claim 69, wherein said step of providing a first level of a semiconductor device comprises providing a first level further comprising at least one conductive structure.

71. A method of processing a portion of a device including a higher horizontal surface, a lower horizontal surface, and a non-horizontal surface, said method comprising:

providing an oxide in a non-conformal manner over said higher horizontal surface, said lower horizontal surface, and said non-horizontal surface; and

introducing an impurity into said oxide.

72. The method in claim 71, wherein said step of providing an oxide in a non-conformal manner comprises providing an oxide having a first thickness on said higher horizontal surface, a second thickness on said lower horizontal surface, and a third thickness on said non-horizontal surface, wherein said first, second, and third thicknesses are different.

73. The method in claim 72, wherein said step of providing an oxide comprises providing an oxide having a first thickness greater than said second thickness.

74. The method in claim 72, wherein said step of providing an oxide comprises providing an oxide having a second thickness greater than said first thickness.

75. The method in claim 74, wherein said step of providing an oxide in a non-conformal manner comprises reacting methylsilane and hydrogen peroxide in an environment including a substrate having a temperature of about 20°C.

76. The method in claim 75, wherein said step of providing an oxide comprises providing an oxide over a non-horizontal surface connecting said higher horizontal surface to said lower horizontal surface.

77. A method of forming a doped oxide over a substrate, comprising:

reacting a methylsilane with hydrogen peroxide proximate said substrate;

forming an oxide from a product of said methylsilane and said hydrogen peroxide; and

introducing a dopant into said oxide.

78. The method in claim 77, wherein said reacting step comprises reacting said hydrogen peroxide with a selection comprising dimethylsilane, trimethylsilane, tetramethylsilane, pentamethyldisilane, and combinations thereof.

79. A semiconductor device, comprising:

a first portion of doped porous oxide on a first surface of said semiconductor device, wherein said first portion of doped oxide has a first thickness; and

a second portion of doped porous oxide on a second surface of said semiconductor device, wherein said second portion has a second thickness different from said first thickness.

80. The device in claim 79, wherein said first surface defines a first plane at a first elevation, and wherein said second surface defines a second plane at a second elevation.

81. The device in claim 80, wherein said first surface defines a first horizontal surface, and wherein said second surface defines a second horizontal surface.

82. The device in claim 81, further comprising a third portion of doped porous oxide on a third surface of said semiconductor device, wherein said third portion has a third thickness different from said first and second thickness.

83. The device in claim 83, wherein said third surface defines a transition from said first surface to said second surface.

84. A material for a portion of a semiconductor device, wherein said portion defines a varying topography, said material comprising a boron-doped porous oxide having varying thicknesses over said portion.

85. The material in claim 84, wherein said oxide is thicker at a higher elevation of said portion than at a lower elevation of said portion.

86. The material in claim 85, wherein said oxide is thicker at a horizontal section of said portion than at a non-horizontal section of said portion.

87. The material in claim 86, wherein said oxide has a thickness of zero at at least a part of said non-horizontal section.

88. The material in claim 87, wherein said oxide has a thickness of zero at said lower elevation.

Abstract of the Disclosure

In a DRAM fabrication process, a first oxide is provided over a transistor gate and over a substrate extending from under the gate. The deposition is non-conformal in that the oxide is thicker over the gate and over the substrate than it is on the side of the gate. A second non-conformal oxide is provided over the first non-conformal oxide. The second oxide is annealed in a boron-containing atmosphere, and the first oxide prevents boron diffusion from the second oxide into the gate and substrate. The second oxide may then serve as an etch stop, a CMP stop, or both.

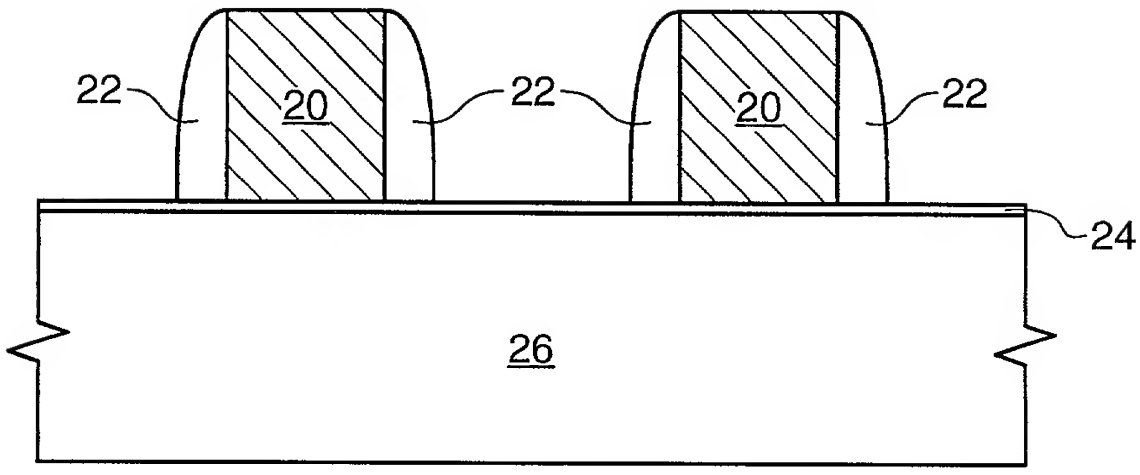

FIG. 1
(PRIOR ART)

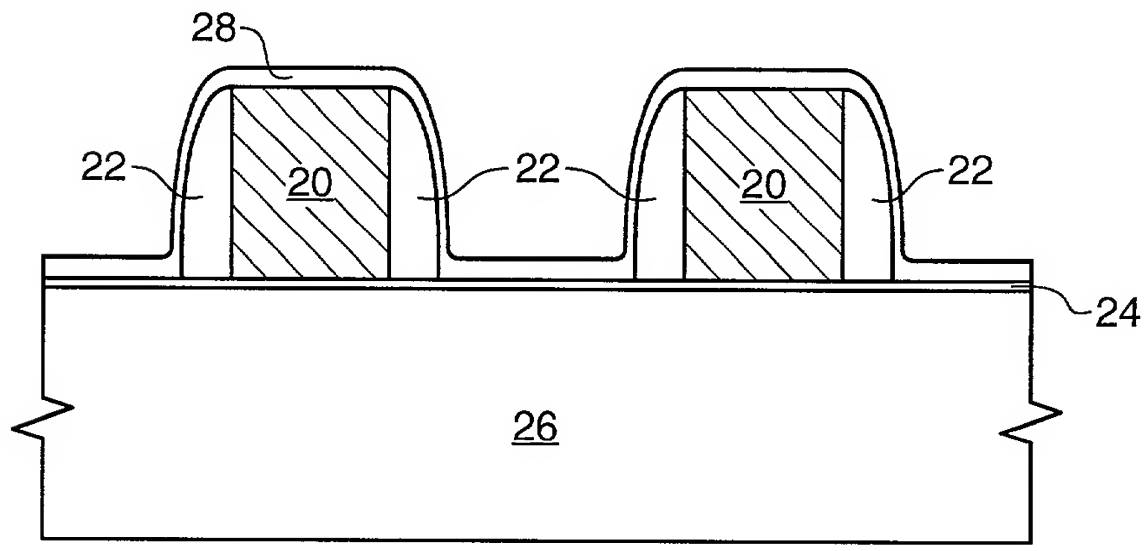

FIG. 2

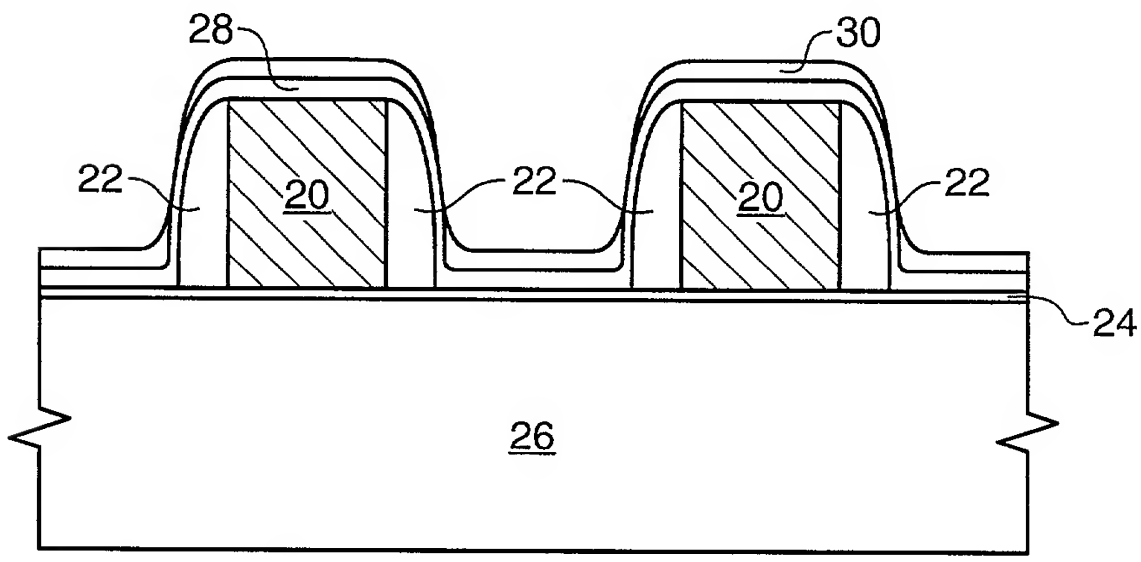

FIG. 3

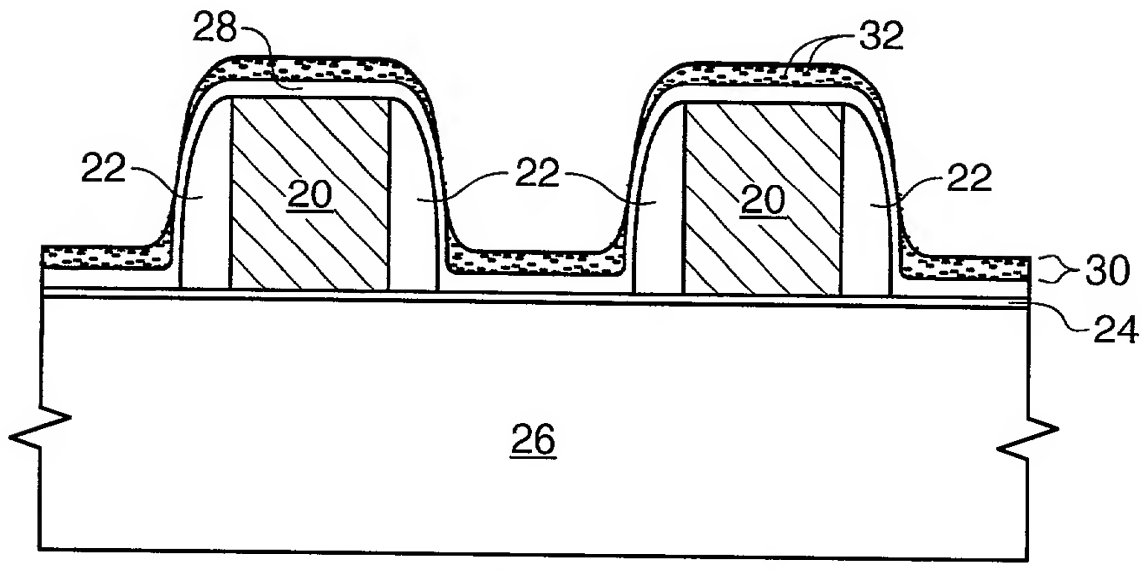

FIG. 4

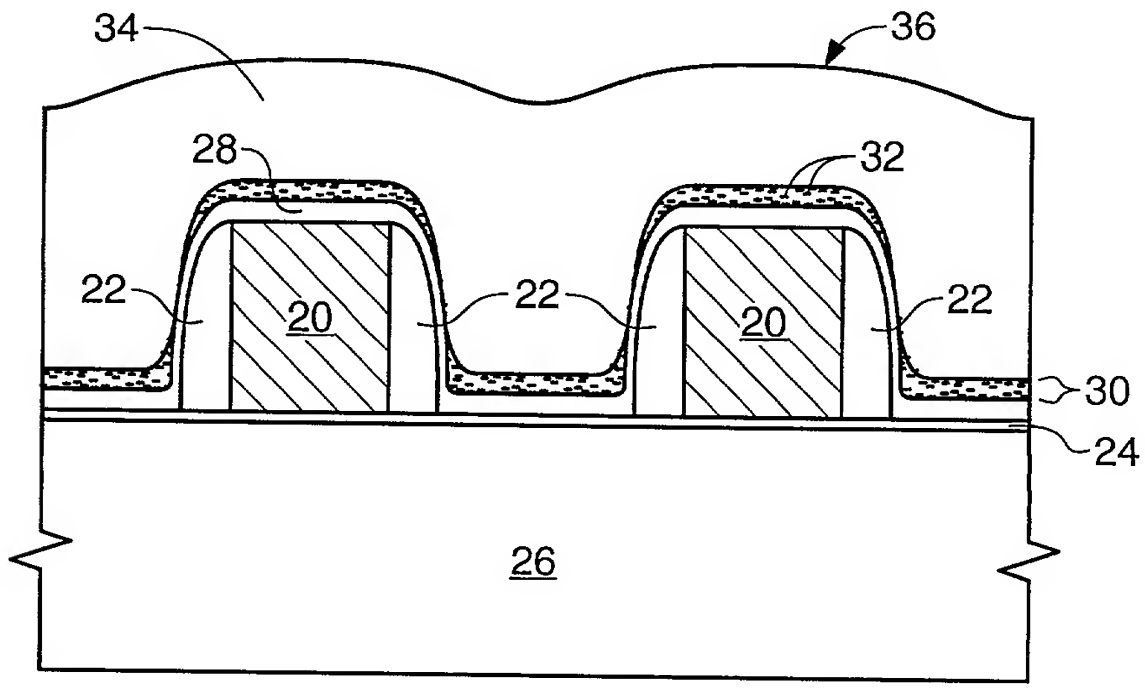

FIG. 5

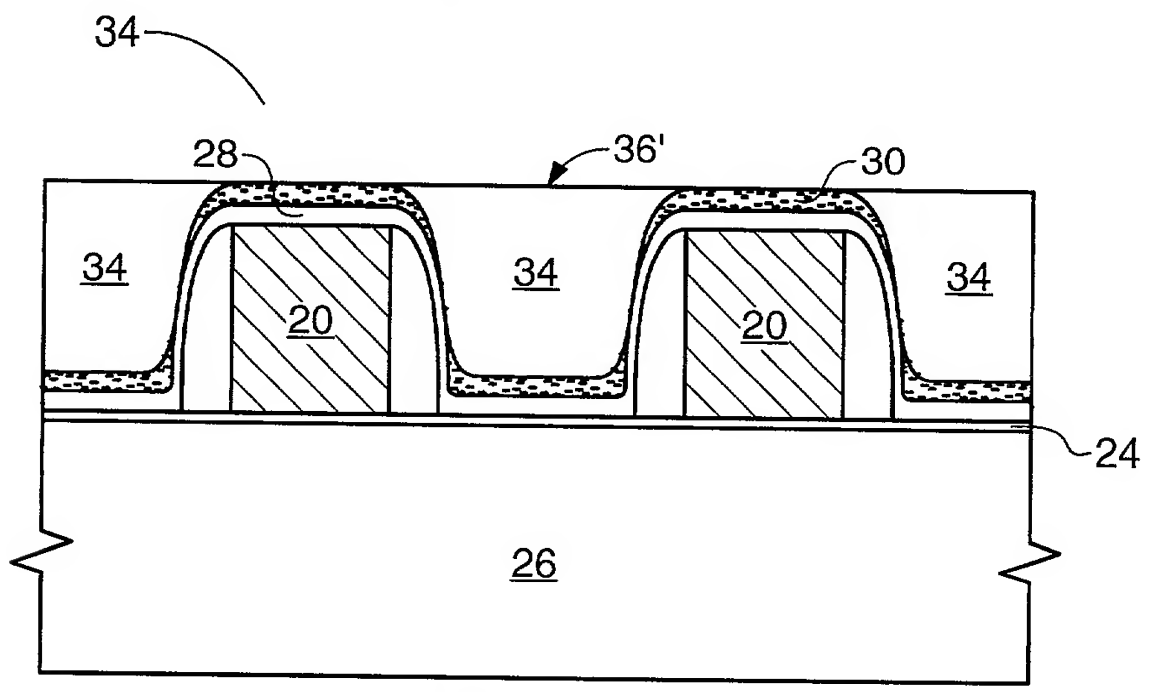

FIG. 6

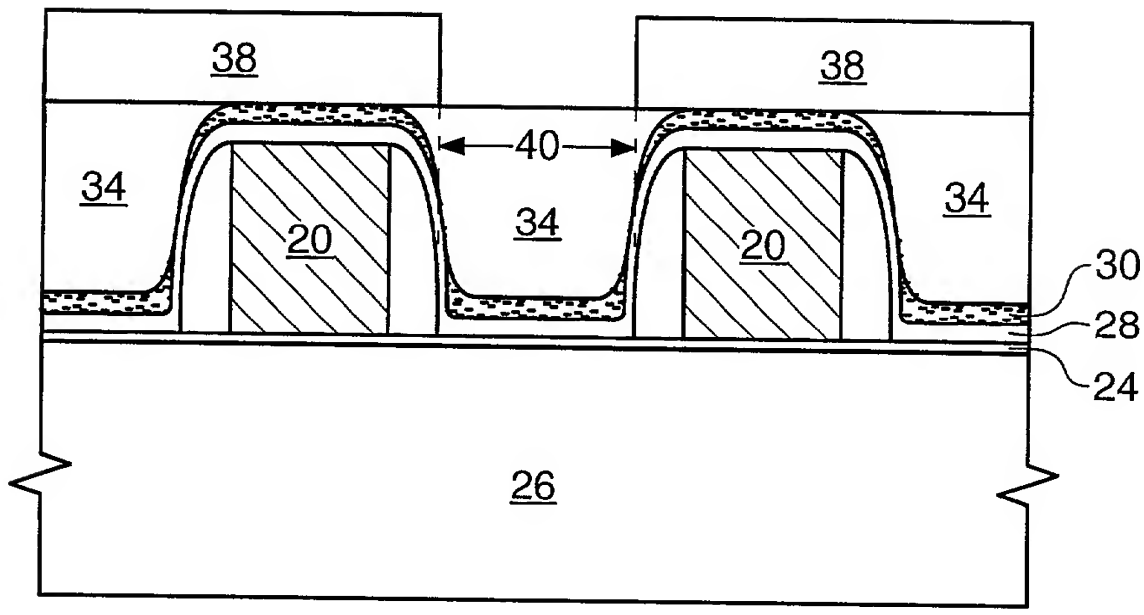

FIG. 7

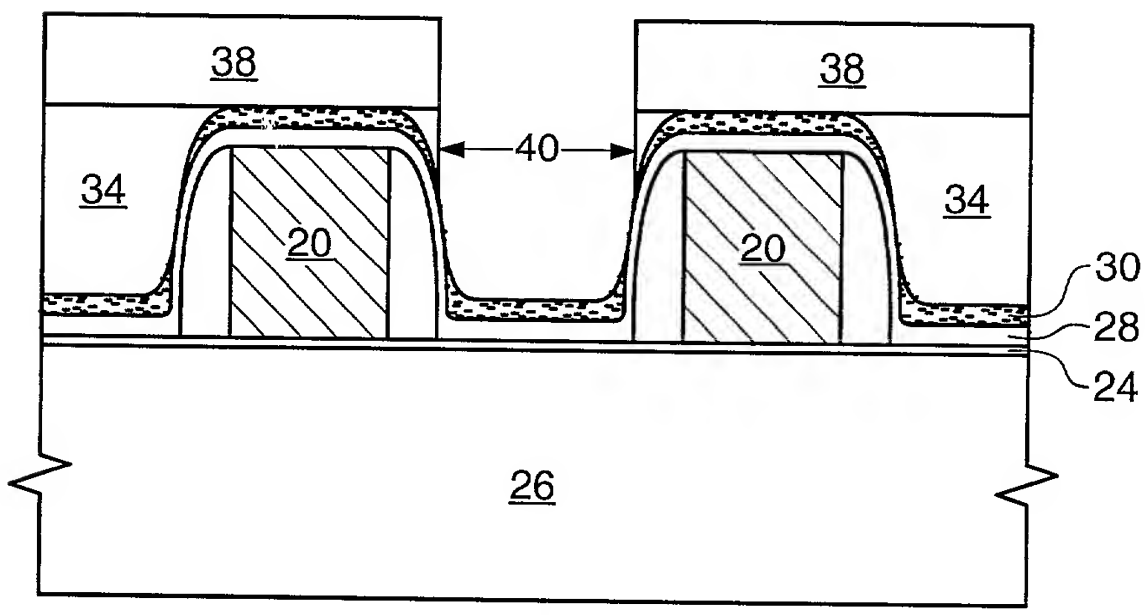

FIG. 8

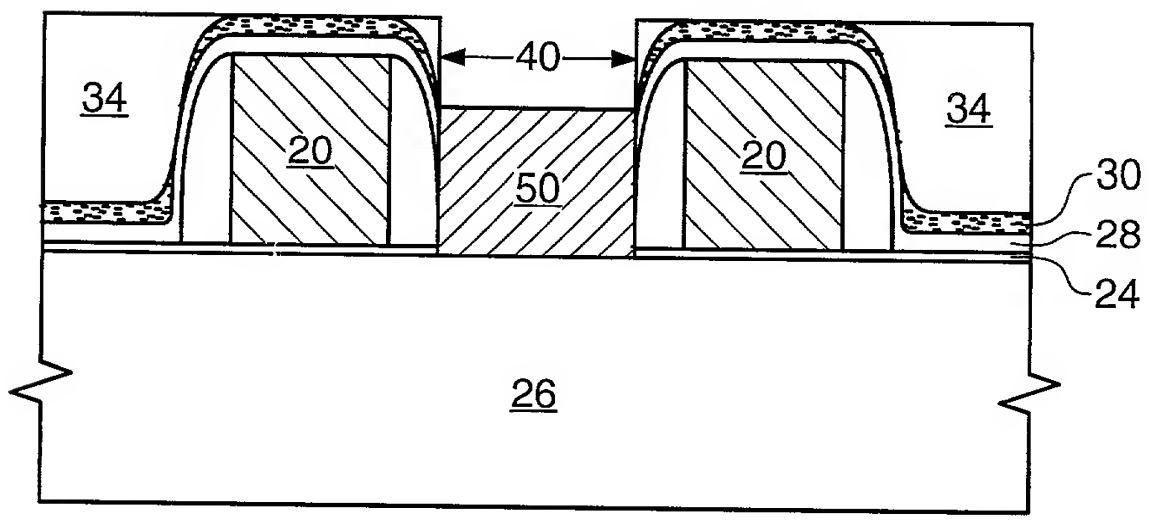

FIG. 9

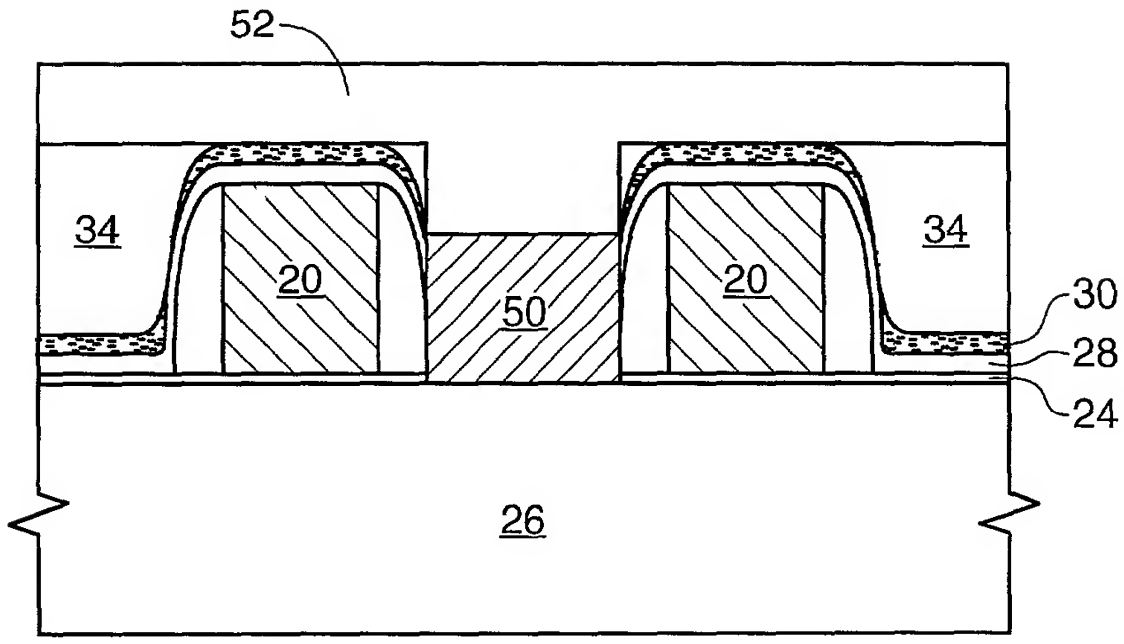

FIG. 10

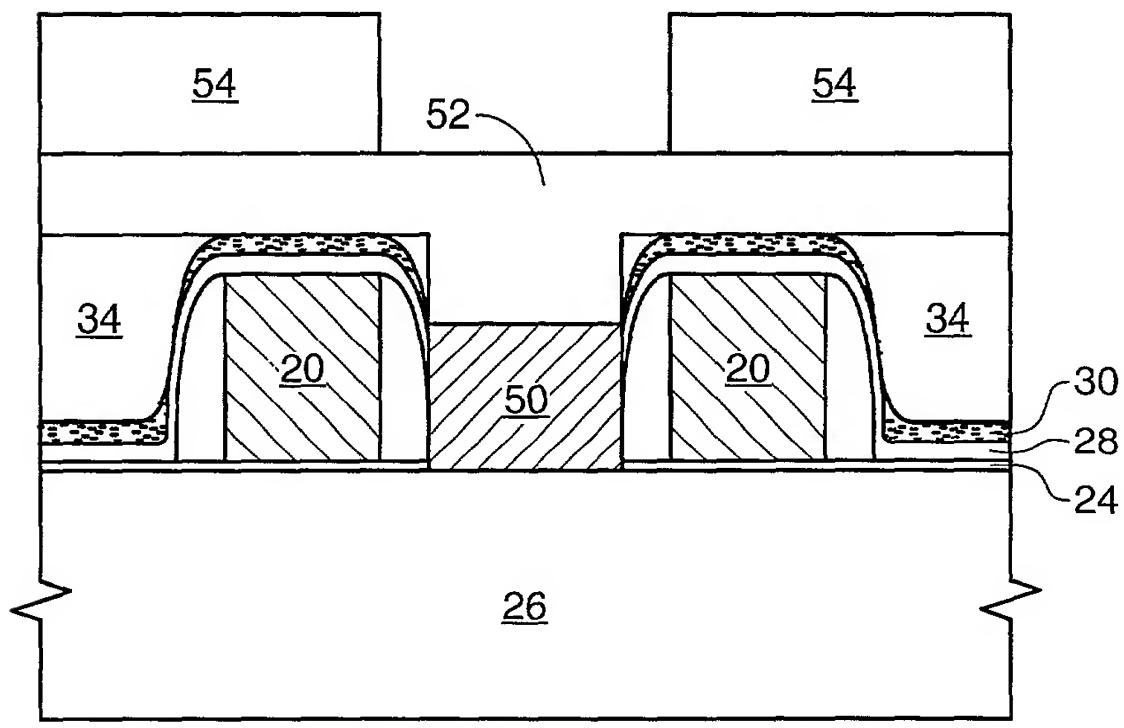

FIG. 11

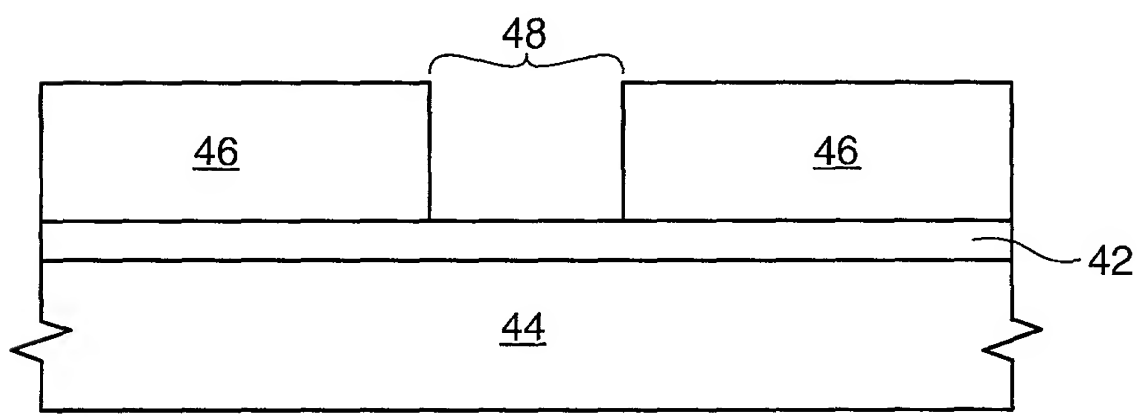

FIG. 12

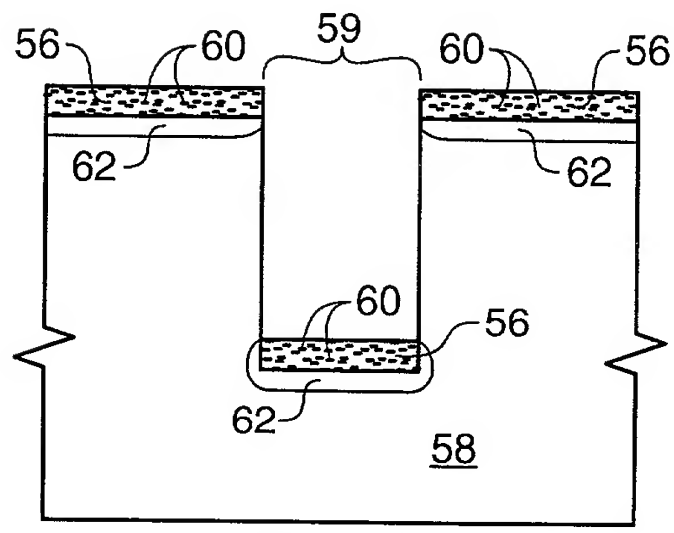

FIG. 13

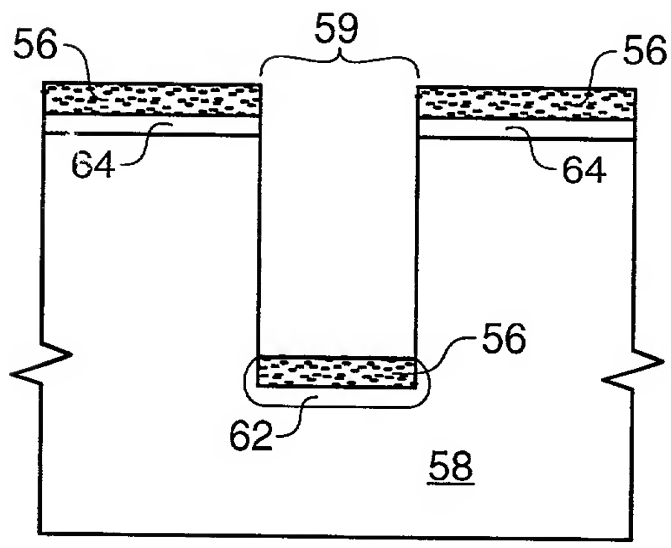

FIG. 14

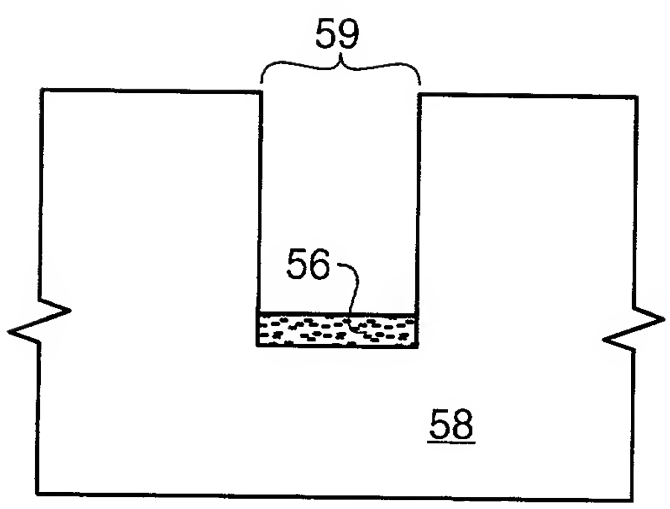

FIG. 15

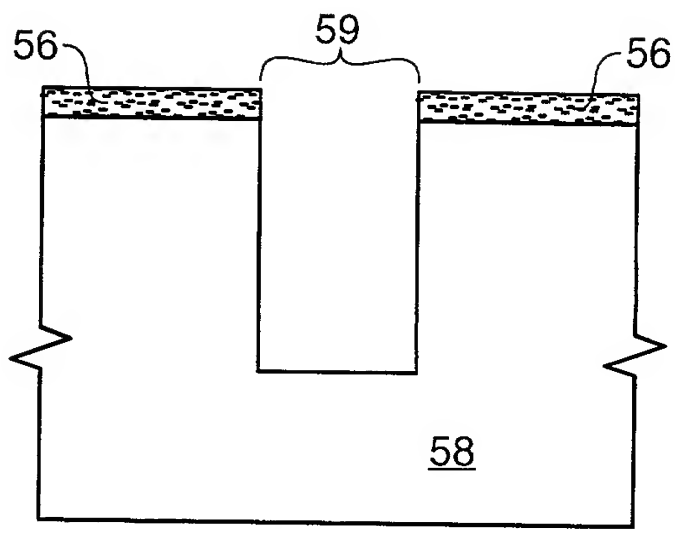

FIG. 16

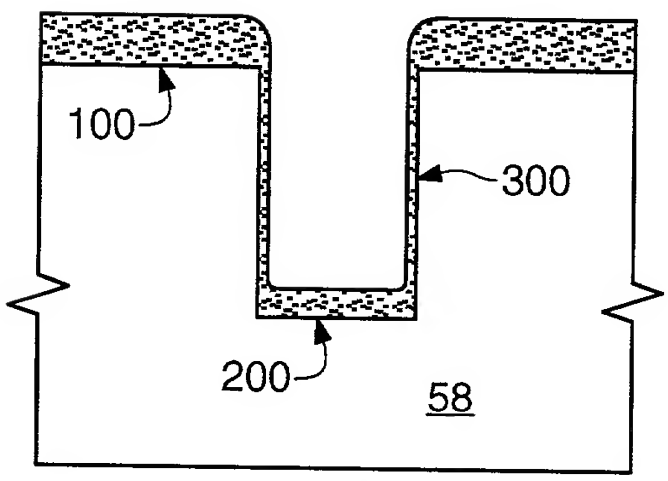

FIG. 17

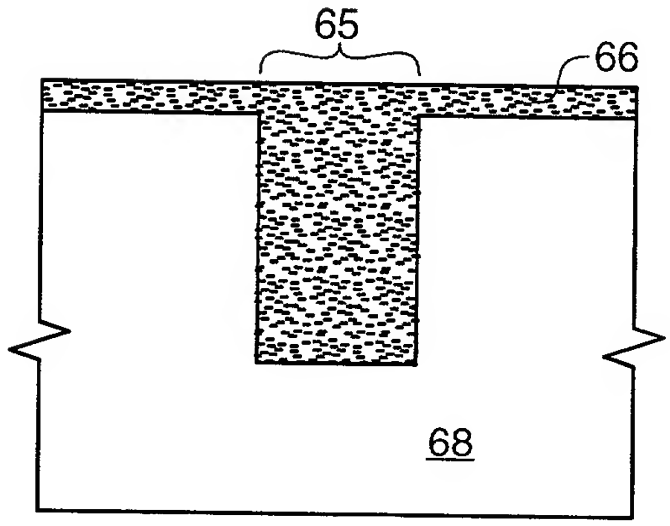

FIG. 18